ZDSD01G/02G/04G/08G/16G/32G/64G

SD NAND

1. Introduction

Zetta SD NAND is an embedded storage solution designed in a LGA8 package form. The operation of SD NAND is similar to an SD card which is an industry standard.

SD NAND consists of NAND flash and a high-performance controller. 3.3V supply voltage is required for the NAND area (VCC). SD NAND is fully compliant with SD2.0 interface, which is utilized by most of general CPU. The advantages of the SD NAND include high quality, low power consumption and cost performance.

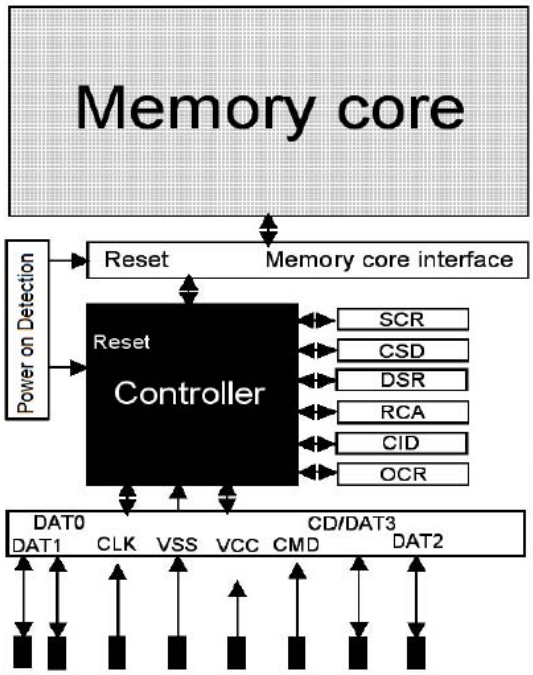
2.Product List

Capacity	Part number	Package	Size	Temp. Range
1Gb (SLC)	ZDSD01GLGEAG	LGA8 (Land Grid Array)	8x6mm	-25° C to +85° C
2Gb (SLC)	ZDSD02GLGEAG	LGA8 (Land Grid Array)	8x6mm	-25° C to +85° C
4Gb (SLC)	ZDSD04GLGEAG	LGA8 (Land Grid Array)	8x6mm	-25° C to +85° C
8Gb (MLC)	ZDSD08GLGEAG	LGA8 (Land Grid Array)	8x6.2mm	-25° C to +85° C
16Gb (MLC)	ZDSD16GLGEAG	LGA8 (Land Grid Array)	8x6.2mm	-25° C to +85° C
32Gb (MLC)	ZDSD32GLGEAG	LGA8 (Land Grid Array)	8x6.2mm	-25° C to +85° C
64Gb (MLC)	ZDSD64GLGEAG-R	LGA8 (Land Grid Array)	8x6.2mm	-25° C to +85° C
1Gb (SLC)	ZDSD01GLGIAG	LGA8 (Land Grid Array)	8x6mm	-40° C to +85° C
2Gb (SLC)	ZDSD02GLGIAG	LGA8 (Land Grid Array)	8x6mm	-40° C to +85° C
4Gb (SLC)	ZDSD04GLGIAG	LGA8 (Land Grid Array)	8x6mm	-40° C to +85° C
8Gb (MLC)	ZDSD08GLGIAG	LGA8 (Land Grid Array)	8x6.2mm	-40° C to +85° C
16Gb (MLC)	ZDSD16GLGIAG	LGA8 (Land Grid Array)	8x6.2mm	-40° C to +85° C
32Gb (MLC)	ZDSD32GLGIAG	LGA8 (Land Grid Array)	8x6.2mm	-40° C to +85° C
64Gb (MLC)	ZDSD64GLGIAG-R	LGA8 (Land Grid Array)	8x6.2mm	-40° C to +85° C

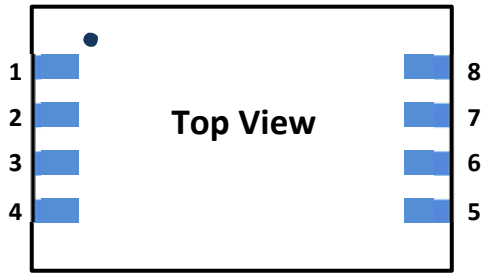
3. Features

- √ Support up to 50Mhz clock frequency
- √ Support 1/4 bit mode
- √ Built-in HW ECC Engine and highly reliable NAND management mechanism
- √ High Speed model, Speed class 4/class 6/class 8/class10 supported.
- √ Smaller package LGA8 (Land Grid Array)
- √ Operation Conditions Temperature Range: Extended Ta = -25° C to +85° C
  Industrial Ta = -40° C to +85° C
- √ Storage Conditions Temperature Range: Tstg = -65° C to +150° C

4. Block Diagram



5. Pin Assignments



Pin No.	Pin name (SD mode)	Pin name (SPI mode)
1	SD2, I/O pin	NC, no connection
2	SD3, I/O pin	/CS, chip select
3	CLK, clock signal	CLK, clock signal
4	Vss, ground	Vss, groud
5	CMD, command signal	DI, data in
6	SD0, I/O pin	DO, data out
7	SD1, I/O pin	NC, no connection
8	Vdd, power supply	Vdd, power supply

6. Usage

6.1. Product Protocol

As SD NAND is the realize SD2.0 standard product, thus please refer to the SD2.0 related protocol: SD Physical Layer Specification Version 2.00.

6.2. DC Characteristics

Item		Symbol	MIN	MAX	Unit	Note
Supply voltage		V_{DD}	2.7	3.6	V	
Input voltage	High Level	V_{IH}	V_{DD}*0.625	V_{DD}+0.3	V	
	Low Level	V_{IL}	V_{SS}-0.3	V_{DD}*0.25	V	
Output voltage	High Level	V_{OH}	V_{DD}*0.75	--	V	I_{OH}=-2mA, V_{DD}=VDDmin
	Low Level	V_{CL}	--	V_{DD}*0.125	V	I_{OL}=2ma, V_{DD}=VDDmin
Standby Current(*)		Icc1	--	20*	mA	V_{DD}=3.6V, clock 25MHz
			--	0.2		V_{DD}=3.0V, clock STOP, Ta=25° C
Operation Current(*)	Write	I	--	25	mA	3.6V/25MHz,50MHz
	Read	I	--	25		
Input voltage setup Time		Vrs	--	250	ms	

Note: Standby current max 20mA with CLOCK 25Mhz only based on 100 pcs samples

Peak Voltage and Leak Current

Item	Symbol	MIN	MAX	Unit	Note
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
Input Leakage Current for all pins		-10	10	uA	
Output Leakage Current for all outputs		-10	10	uA	

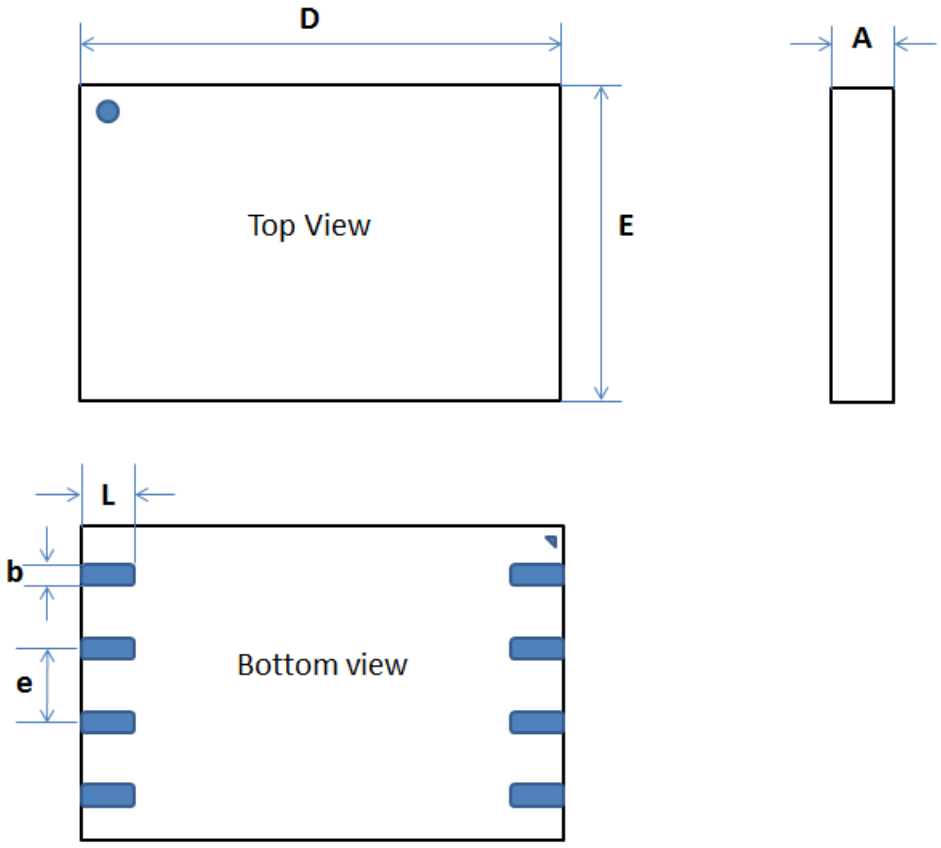
Signal Capacitance

Pull up Resistance	R_{CMD}/R_{DAT}	10	100	k	
Total bus capacitance for each signal line	C_L	-	40	pF	1 card $C_{HOST}+C_{BUS}\leqslant 30pF$
Card Capacitance for signal pin	C_{CARD}	-	10	pF	
Pull up Resistance inside card (pin1)	R_{DAT3}	10	90	k	
Capacity Connected to Power line	C_C	-	5	pF	

Note: WP pull-up (Rwp) Value is depend on the Host Interface drive circuit.

7. Package Dimensions

LGA8 (SLC 8x6mm/MLC 8x6.2mm) (Land Grid Array)

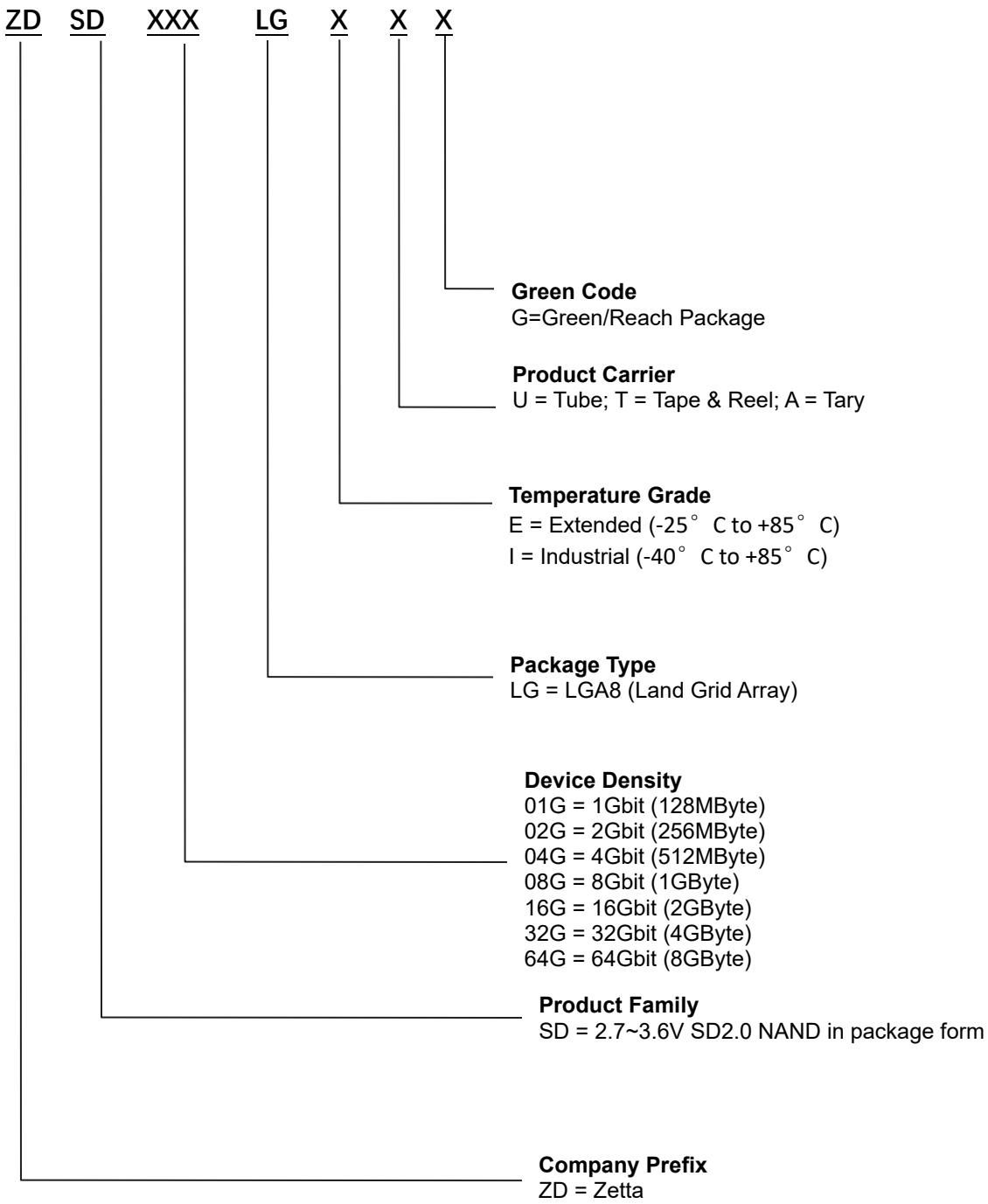


Dimensions:

Symbol / Unit		A	b	D	E-SLC	E-MLC	e	L
Mm	Min	0.75	0.55	7.95	5.90	6.10		0.75
	Norm	0.80	0.60	8.00	6.00	6.20	1.27	0.80
	Max	0.85	0.65	8.05	6.10	6.30		0.85

8. Ordering Information

The ordering part number is formed by a valid combination of the following



9. Revision History

Version No.	Change Description	Date
V1.0	Initial release, part number is based on SLC Nand, LGA 8*6mm	2020/06/02
V1.1	Add MLC SD Nand and LGA 8*6.2mm package	2021/12/01
V1.2	Ordering Information Update	2022/2/20
V1.3	Add 64Gb MLC SD Nand	2022/10/08

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