Key Design Features

- Synthesizable IP Core for Xilinx® FPGA 7-series and later (other FPGA devices and vendors supported on request)

- Supplied as human-readable RTL source code

- Compatible with all Sony® FCB-EV Series LVDS video cameras such as the FCB-EV7520 and FCB-EV7320 models

- Support for HD1080p60 (double-mode) and HD1080p30 (single-mode) operation (other modes supported on request)

- Choice of 8 x LVDS data lanes or 4 x LVDS data lanes

- Generates a standard SMPTE 274M output video stream

Applications

- Simple connectivity to the Sony® FCB-EV series HD-cameras

- Easily adaptable for other LVDS cameras

- Replacement for the Thine® THC63LVD series or the Rohm® BU90R series LVDS receiver ICs recommend by Sony

Pin-out Description

| Pin name	I/O	Description	Active state
RESET_N	in	Asynchronous reset	low
CAM_TXCLKOUT_P CAM_TXCLKOUT_N	in	LVDS input clock (74.25 MHz nominal)	LVDS differential
CAM_TXOUT*_P CAM_TXOUT*_N	in	LVDS input data lanes (4-lanes single-mode) (8-lanes double-mode	LVDS differential
SMPTE_LOCK	out	Indicates that receiver has locked to the SMPTE video stream	high
SMPTE_PCLK	out	Pixel clock output (148.5 MHz)	synchronous clock
SMPTE_TCLK	out	Camera clock output (74.25 MHz)	synchronous clock
SMPTE_SCLK	out	Serial clock output (519.75 MHz)	synchronous clock
SMPTE_DATA	out	Standard SMPTE 274M data stream out (1080p30 or 1080p60 video)	16-bit data (single-mode 1 pixel/clock) 32-bit data (double-mode 2 pixels/clock)
SMPTE_SOF	out	Start of Frame flag (first pixel active frame)	high
SMPTE_SOL	out	Start of Line flag (first pixel active line)	high
SMPTE_DE	out	Data Enable flag (active video is valid)	high

Block Diagram
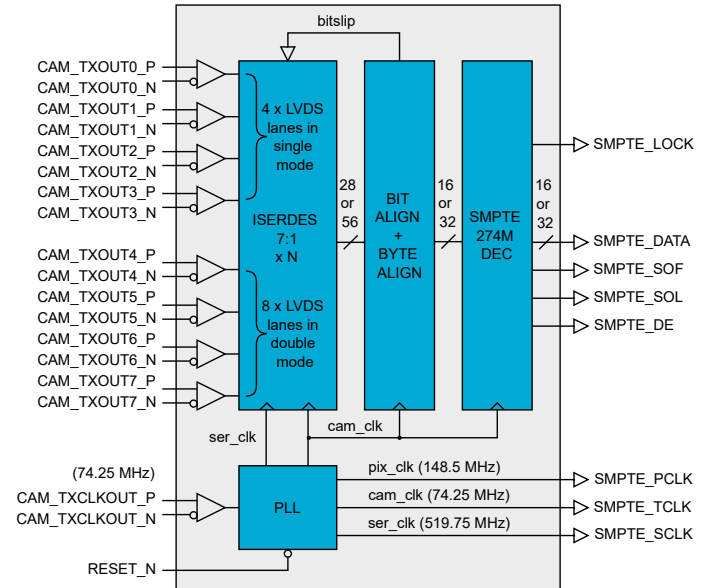
Figure 1: Sony LVDS camera interface (internal architecture)

General Description

The SONY_CAM_IF IP Core (Figure 1) provides a simple way to connect the Sony® FCB-EV range of cameras to your FPGA. It serves as a direct replacement for an external LVDS receiver IC and takes advantage of the fast LVDS I/O solutions provided by modern FPGA devices.

The interface supports both single-mode and double-mode operation in which 4 x LVDS data lanes or 8 x LVDS data lanes may be connected to the IP Core. In the standard configuration, the camera input clock (TXCLKOUT_P/N) is assumed to be set to a frequency of 74.25 MHz. This permits operation at HD1080p30 resolution in *single-mode* (1x16-bit pixels per clock) or HD1080p60 operation in *double-mode* (2x16-bit pixels per clock)[1].

The LVDS data lanes are deserialized using the high-speed SERDES input resources of the FPGA.. The resulting parallel data are then aligned and decoded to provide a standard SMPTE 274M output video stream. SMPTE data changes on the rising-clock edge of the SMPTE_TCLK (cam_clk) signal.

Other flags are also provided to indicate the presence of active video, the start of an active frame and the start of an active line. In addition, there is a stream locked flag that indicates the bit alignment has succeeded and a valid SMPTE stream has been found.

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1   Full details on the camera modes of operation can be found in the Sony FCB-EV series datasheet. Other clocking options and video resolutions may be provided on request.

Data Sampling Considerations

The internal clocking is provided by the PLL resources of the FPGA. The PLL receives the 74.25 MHz camera LVDS input clock and generates three further clocks which are are *pix_clk, cam_clk* and *ser_clk*. These clocks are also made available at the outputs of the IP Core as shown by Figure 1 above. All three clocks are synchronous with the output SMPTE data stream and the camera clock input.

Normally the user will use the *cam_clk* (SMPTE_TCLK) output as the SMPTE parallel data is latched on the rising-edge of this clock. The other clocks may also be used by the downstream interface if required. If not, they may be left unconnected in the implementation.

One critical thing to take into account when designing with the camera interface is to set the correct phase for the serial clock. The serial clock is the clock used to sample the incoming LVDS bitstream. By modifying the phase of this clock, then the sample point within the data 'eye' is changed. This is shown graphically in Figure 2 below.
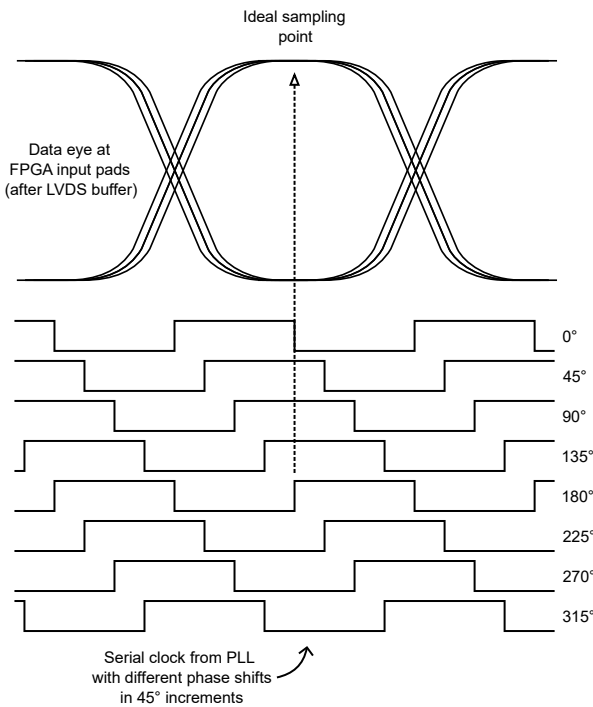

Figure 2: Serial sampling clock relative to the data 'eye'

Depending on the physical characteristics of the PCB and the physical properties of the LVDS routing then it may be necessary to modify the phase accordingly. The ultimate goal is to try and position the sample point in the middle of the data eye. To this end, the PLL in the FPGA allows the phase to be shifted by 45 degree steps.

By default, the design has an 180° phase shift on the serial clock. This, in principle, should mean the rising-edge appears directly in the middle of the eye. However, some experimentation may be required to achieve the best possible results.

Functional Timing

The input timing of the LVDS camera interface corresponds exactly to the Sony datasheet. For single-mode operation, the Y and C component values are serialized as shown in Figure 3 below. After deserialization, the output is 1 x 16-bit YcbCr 4:2:2 pixel per clock.
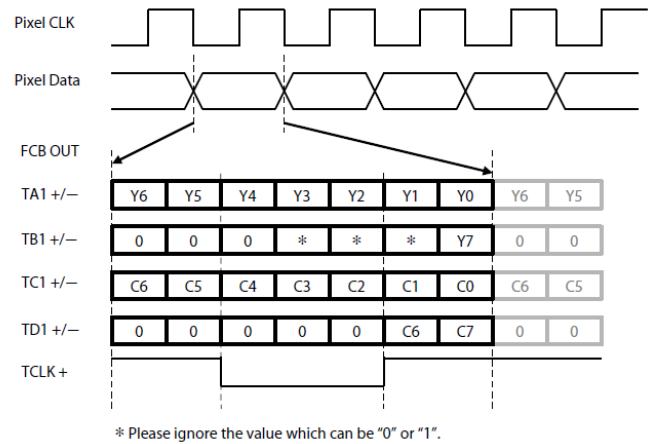

Figure 3: Sony camera single-mode pixel format

The input timing for double-mode is identical save for the fact that 2 x 16-bit pixels are processed and serialized in parallel. The output after deserialization is therefore 2 x 16-bit YcbCr 4:2:2 pixles per clock. Figure 4 shows the timing waveforms.
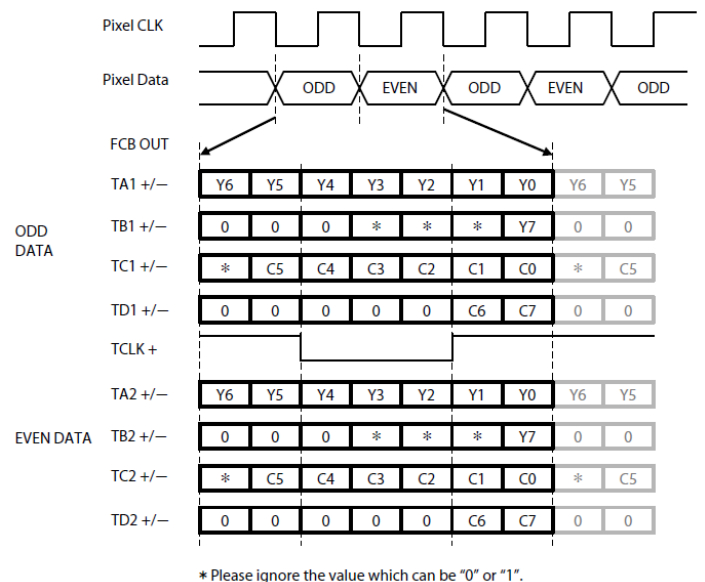

Figure 4: Sony camera double-mode pixel format

The SMPTE output data timing for single mode is shown below in Figure 5. This timing diagram shows the output video at the start of an active frame when 'SOF' is active. The timing waveforms are identical at the start of an active line, with the exception that the 'SOF' flag is low.

Likewise, the SMPTE output data timing for double-mode operation is identical to single-mode with the exception that 2 x 16-bit pixels are generated per clock cycle. The YCbCr data is output as 32-bits in the format: Y_odd/Y_even/C_odd/C_even.
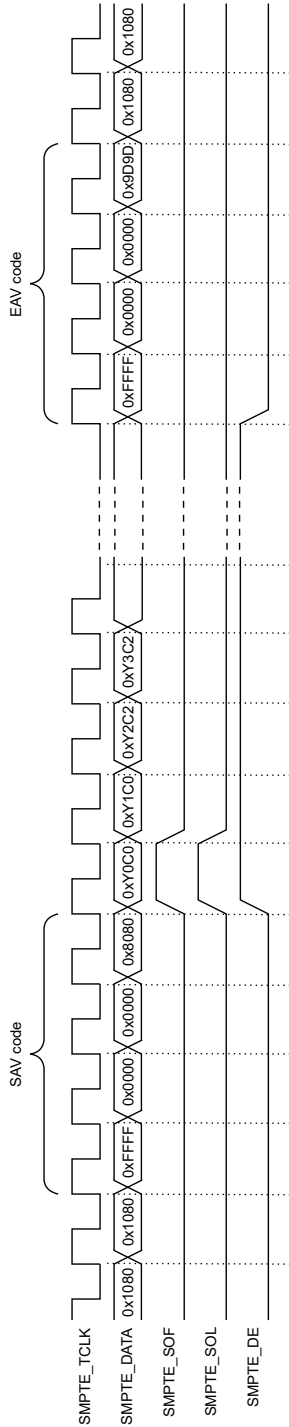

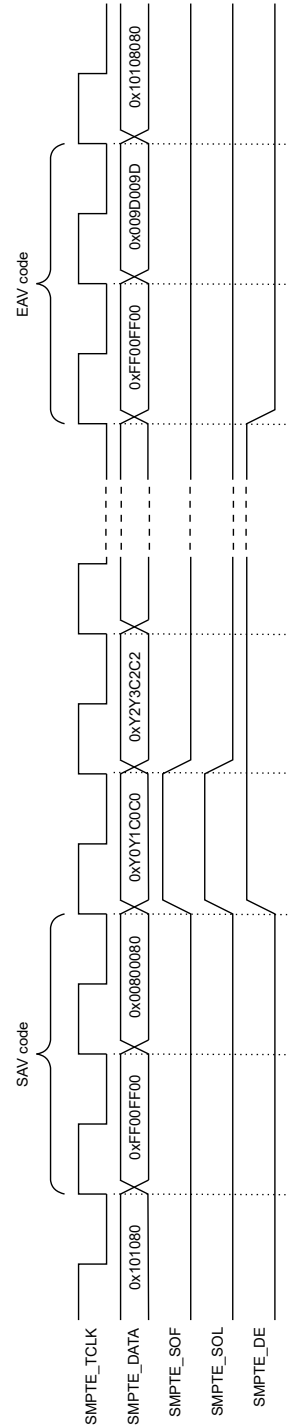*Figure 5: SMPTE
(single-mode)
output data timing*

*Figure 6: SMPTE
(double-mode)
output data timing*

Source File Description

All source files are provided as text files coded in VHDL. The exception is the Xilinx hard-IP that is only available in Verilog. The following table gives a brief description of each file for both single-mode and double-mode implementations.

SINGLE-MODE

Source file	Description
glbl.v	Xilinx global definitions
xilinx7_iserdes.v	Xilinx ISERDES hard IP
xilinx7_iserdes_pll_clk.v	Xilinx PLL hard IP
sony_cam_reset_retime.vhd	Async reset retiming module
sony_cam_bit_align.vhd	Bit alignment controller
sony_cam_smpte_dec16.vhd	SMPTE stream decoder (16-bit)
sony_cam_test_pattern.vhd	Simple test pattern for debug only
sony_cam_tpg_1080p.vhd	SMPTE 274M test pattern generator
sony_cam_if_single.vhd	Top-level (single-mode) component
sony_cam_if_single_bench.vhd	Top-level test bench

DOUBLE-MODE

Source file	Description
glbl.v	Xilinx global definitions
xilinx7_iserdes.v	Xilinx ISERDES hard IP
xilinx7_iserdes_pll_clk.v	Xilinx PLL hard IP
sony_cam_reset_retime.vhd	Async reset retiming module
sony_cam_bit_align.vhd	Bit alignment controller
sony_cam_byte_align.vhd	Byte alignment controller
sony_cam_smpte_dec32.vhd	SMPTE stream decoder (32-bit)
sony_cam_test_pattern.vhd	Simple test pattern for debug only
sony_cam_tpg_1080p.vhd	SMPTE 274M test pattern generator
sony_cam_if_double.vhd	Top-level (double-mode) component
sony_cam_if_double_bench.vhd	Top-level test bench

Functional Testing

An example VHDL testbench is provided for use in a suitable hardware simulator such as Modelsim® from Mentor Graphics.. There are separate test benches for the single-mode and double-mode components. In the example testbench, a simple SMPTE 1080p test pattern is generated as an input to the Sony camera interface IP Core.

In single-mode, the simulation must be run for at least 34 ms which is enough time for one frame of 1080p30 video.. In double-mode, then 17 ms is sufficient for one frame of 1080p60. During the simulation, the output SMPTE stream is captured in a file called *smpte_out16.txt* or smpte_out32.txt depending on whether the simulation is in single or double mode.

The video output of the simulation is shown in Figure 7 which is a series of greyscale vertical bars.
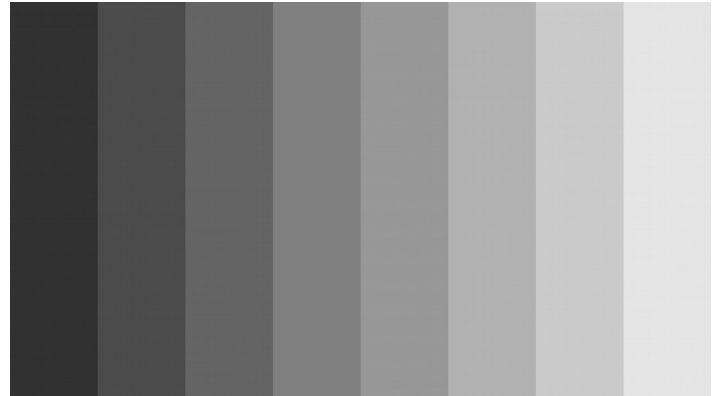

Figure 7: Output test image generated by the Sony Camera interface simulation

Synthesis and Implementation

The files required for synthesis and the design hierarchy is shown below:

- sony_cam_if_single.vhd
    - xilinx7_pll_clk.v
    - xilinx7_iserdes.v
    - sony_cam_reset_retime.vhd
    - sony_cam_bit_align.vhd
    - sony_cam_smpte_dec16.vhd

- sony_cam_if_double.vhd
    - xilinx7_pll_clk.v
    - xilinx7_iserdes.v
    - sony_cam_reset_retime.vhd
    - sony_cam_bit_align.vhd
    - sony_cam_byte_align.vhd
    - sony_cam_smpte_dec32.vhd

In the standard form, the IP Core is designed for use with the Xilinx® 7-series range of FPGAs. However, small modifications can be made to the IP Core to make it compatible with other vendors and technologies. Please contact Zipcores for further information.

Example physical and timing constraints are provided as a Xilinx *xdc* file. These constraints have been chosen for a Xilinx Artix-7 FPGA. Careful choice of FPGA pin connections should be made such that the LVDS input pairs are placed locally at the input pads. Failure to do so, could result in significant skew between LVDS data lanes which can affect timing and performance.

Trial synthesis results are shown for Artix-7 in the following tables with resource usage specified after place and route.

XILINX® 7-SERIES FPGAS (SINGLE-MODE)

Resource type	Artix-7
Slice Register	162
Slice LUTs	105
Block RAM	0
DSP48	0
ISERDES	4
IBUFDS	5
MMCME2_ADV	1
Occupied Slices	50
Clock freq. (approx)	74.25 MHz (default) or 148.5 MHz

XILINX® 7-SERIES FPGAS (DOUBLE-MODE)

Resource type	Artix-7
Slice Register	253
Slice LUTs	222
Block RAM	0
DSP48	0
ISERDES	8
IBUFDS	9
MMCME2_ADV	1
Occupied Slices	84
Clock freq. (approx)	74.25 MHz (default) or 148.5 MHz

Revision History

Revision	Change description	Date
1.0	Initial revision	03/05/2019
1.1	First official release	13/05/2019

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