Key Design Features

- Synthesizable, technology independent IP Core for FPGA, ASIC and SoC
- Supplied as human readable VHDL (or Verilog) source code
- Simple FIFO input interface
- Programmable RGB channel data width (8,10,12,14-bits etc.)
- Highly versatile architecture supports direct connection to a wide range of video DACs, video encoders and DVI/HDMI transmitters
- VSYNC, HSYNC, CSYNC, DE and BLANKING outputs
- Fully programmable timing parameters
- Supports industry standard (VESA, CEA-861, ITU-R BT.656 etc.) and fully custom video modes (both progressive and interlaced formats)
- Future-proof design supports resolutions up to 2^{16} x 2^{16} pixels (8K video and above)
- Independent system and pixel clocks supporting frequencies of 400 MHz+ on basic FPGA platforms[1]
- Compatible with all Zipcores video IP Cores

Applications

- HD, UHD and SUHD next generation digital video
- Legacy (SD) and analogue video applications
- Computer monitors and flat-panel displays
- Digital TV and multimedia solutions

Generic Parameters

Generic name	Description	Type	Valid Range
dw	Pixel data width Pixel data is RGB where 'dw' defines the width in bits of each colour channel	integer	< 2^{16}

Block Diagram

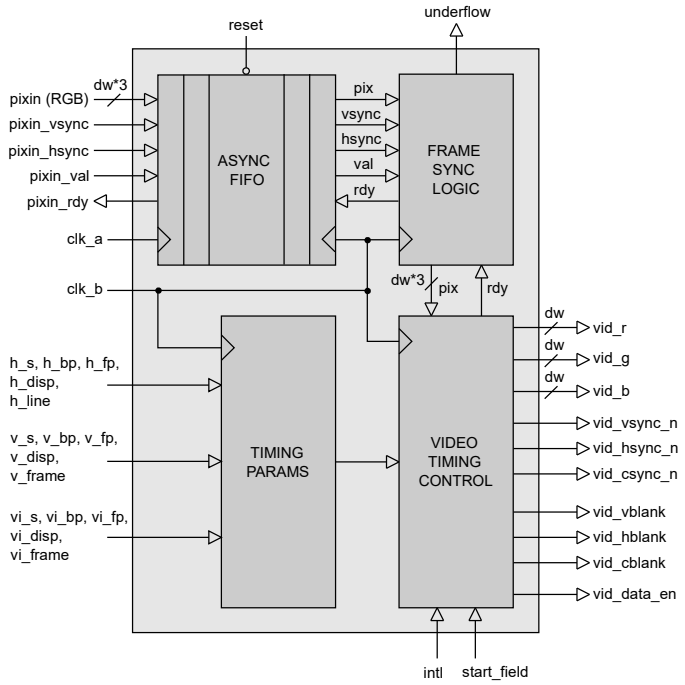


Figure 1: Video timing generator architecture

General Description

The VID_TIMING_GEN IP Core is a fully configurable video timing generator with the ability to support any video resolution up to 2^{16} x 2^{16} pixels in size. The module is compatible with a wide range of video DACs, encoders and transmitters and provides a flexible solution for displaying digital or analogue video on an external TV, monitor or flat panel display. The module is capable of clock speeds in excess of 400 MHz on some FPGA platforms, making it ideal for the latest generation HD and UHD video solutions.

Input pixels and syncs are read on the rising edge of *clk_a* (the system clock) when *pixin_val* and *pixin_rdy* are both active high. The input signal *pixin_vsync* is coincident with the first active pixel in a frame and the signal *pixin_hsync* is coincident with the first active pixel in a line.

(Note that these sync signals should not be confused with true video timing signals. Their purpose is to delineate the first pixel in a frame and the first pixel in a line only).

After resynchronizing the input pixels to the pixel-clock domain (*clk_b*), the controller locks to the first frame (or field) of video. Once frame-lock is achieved, pixels are supplied on demand to the video timing control unit. This module generates the correct RGB video, sync and blanking information depending on the chosen timing parameters.

1 Xilinx® 7-series used as a benchmark

Pin-out Description

Pin name	*I/O*	*Description*	*Active state*
clk_a	in	System clock	rising edge
clk_b	in	Pixel clock	rising edge
reset	in	Asynchronous reset	low
underflow	out	Indicates pixel underflow (synchronized to clk_b)	High

intl	in	Select progressive or interlaced video	0 = progressive 1 = interlaced
start_field	in	Start generating interlaced video on ODD or EVEN field	0 = ODD 1 = EVEN

h_s [15:0]	in	Horizontal sync pulse duration	data
h_bp [15:0]	in	Horizontal back-porch duration	data
h_fp [15:0]	in	Horizontal front-porch duration	data
h_disp [15:0]	in	Active pixels per line	data
h_line [15:0]	in	Duration of whole line	data

v_s [15:0]	in	Vertical sync pulse duration (frame or interlaced field #1)	data
v_bp [15:0]	in	Vertical back-porch duration (frame or interlaced field #1)	data
v_fp [15:0]	in	Vertical front-porch duration (frame or interlaced field #1)	data
v_disp [15:0]	in	Active lines per frame (or interlaced field #1)	data
v_frame [15:0]	in	Duration of whole frame (or interlaced field #1)	data

vi_s [15:0]	in	Vertical sync pulse[2] duration (interlaced field #2)	data
vi_bp [15:0]	in	Vertical back-porch duration (interlaced field #2)	data
vi_fp [15:0]	in	Vertical front-porch duration (interlaced field #2)	data
vi_disp [15:0]	in	Active lines per interlaced field #2	data
vi_frame [15:0]	in	Duration of whole interlaced field #2	data

2 Vertical timing parameters for the interlaced field (vi_* etc.) are ignored and may be tied to zero when generating progressive video.

Pin-out Description cont ...

Pin name	*I/O*	*Description*	*Active state*
pixin [dw*3:0]	in	RGB input pixel	data
pixin_vsync	in	Vertical sync pulse (coincident with first pixel of a frame or field)	high
pixin_hsync	in	Horizontal sync pulse (coincident with first pixel of a line)	high
pixin_val	in	Input pixel valid	high
pixin_rdy	out	Ready to accept input pixel (handshake signal)	high

vid_r [dw - 1:0]	out	Video out RED	data
vid_g [dw - 1:0]	out	Video out GREEN	data
vid_b [dw - 1:0]	out	Video out BLUE	data
vid_vsync_n	out	Video VSYNC	low
vid_hsync_n	out	Video HSYNC	low
vid_csync_n	out	Video CSYNC	low
vid_vblank	out	Video vertical BLANK	high
vid_hblank	out	Video horizontal BLANK	high
vid_cblank	out	Video composite BLANK	high
vid_data_en	out	Video DATA enable	high

Programmable timing parameters

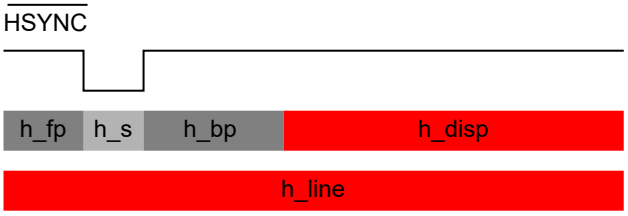
The timing parameters determine the duration of the output video, syncs and blanking. They also determine the relative position of the active video signal between syncs. Timing parameters are specified as an integer number of *pixels* (or pixel clocks) for the horizontal timing. For the vertical timing parameters, values are specified as an integer number of *lines*.

Note that the video timing generator also supports interlaced video formats. For interlaced formats then the signal *intl* must be set to *true*. The input signal *start_field* determines whether the output video begins on field #1 or field #2.

When operating in interlaced mode, then the user must specify the vertical timing information for both fields. Typically, the first field has fewer vertical blanking lines than the second field. When working with progressive video, then the user only needs to specify the vertical timing information for a complete frame. The interlaced timing parameters may be tied off to zero.

All timing parameters are programmable. Whenever the timing parameters are changed during operation, it is advised to reset the module in order to prevent corruption of the video signal.

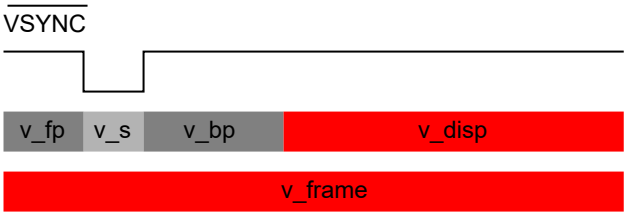
The timing parameters must be specified correctly for the chosen video mode. Figures 2 and 3 on the following page shows this pictorially.



h_fp : Horizontal front-porch
h_s : Horizontal sync
h_bp : Horizontal back-porch
h_disp : Horizontal active display period
h_line : Total number of pixels per line

(N.B. all timing parameters as integer number of pixels)

Figure 2: Horizontal timing parameters



v_fp : Veritcal front-porch
v_s : Vertical sync
v_bp : Vertical back-porch
v_disp : Veritcal active display period
v_frame : Total number of lines per frame

(N.B. All timing parameters as integer number of lines)

Figure 3: Vertical timing parameters

As an example, consider a standard XGA output (1024 x 768) with a screen refresh rate of 60 Hz and a pixel-clock frequency of 65 MHz. The following tables describe the horizontal and vertical timing settings according to the VESA specification.

HORIZONTAL TIMING (XGA at 60Hz)

Generic parameter	***Description***	***Value***
h_fp	Front-porch	24
h_s	Sync pulse	136
h_bp	Back-porch	160
h_disp	Visible area	1024
h_line	Whole line	1344

VERTICAL TIMING (XGA at 60Hz)

Generic parameter	***Description***	***Value***
v_fp	Front-porch	3
v_s	Sync pulse	6
v_bp	Back-porch	29
v_disp	Visible area	768
v_frame	Whole frame	806

By modifying the respective horizontal and vertical timing parameters, a diverse range of standard and fully-custom video modes may be displayed.

Standard video timing output signals

The output video timing signals are compatible with standard off-the-shelf video DACs, encoders and transmitters. In addition to separate VSYNC and HSYNC signals, the module also provides a Composite SYNC signal that is often used to provide sync information on the GREEN channel of the output video.

As well as sync information, the module also provides a video data enable (DE) signal and separate vertical, horizontal and composite blanking outputs. The data enable is high during active pixels. Conversely, the blanking enable(s) are high when active video is not present. The data enable signal is commonly used when interfacing to DVI and HDMI transmitters in order to enable valid pixels into the device.

Pixel input/output rate considerations

During normal operation, it is important to ensure that the input pixel rate is sufficient to sustain the chosen video mode. If at any point, the video timing generator detects an internal buffer underflow, then the *underflow* flag is asserted. Once underflow has occurred, then subsequent pixels will be out of sync and the output display will become corrupted.

The output may be reset by asserting the system reset signal for at least one *clk_a* cycle. This will result in a resynchronization of the video signal and the recovery of a clean video output display within a single frame period.

Functional Timing

Input video timing

RGB pixels are sampled at the module input according to the valid-ready pipeline protocol. Figure 4 shows the signalling at the input of the video signal generator at the start of a new frame. The first pixel of a new frame begins with *pixout_vsync* and *pixout_hsync* asserted high together with the first pixel. Note that when *pixin_rdy* is asserted low, then input pixels must be held-off, otherwise pixels with be lost and the output video will become out of sync[3].

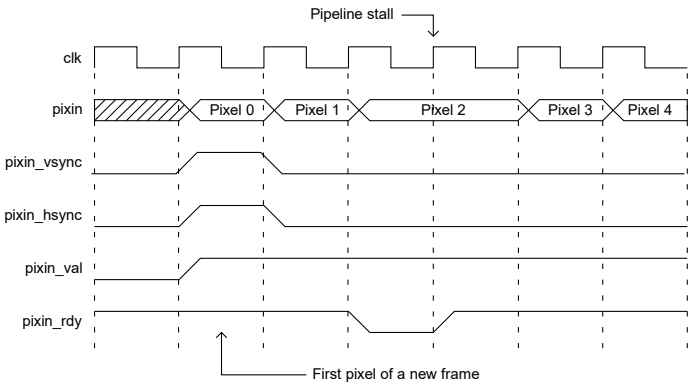


Figure 4: First input pixel in a frame

For the first pixel in a new line (Figure 5) the signal *pixout_hsync* is asserted high with *pixout_vsync* held low. Note that as well as a pipeline stall, Figure 5 also shows an invalid pixel condition. When *pixin_val* is low, the input pixel and input syncs (if present) are ignored.

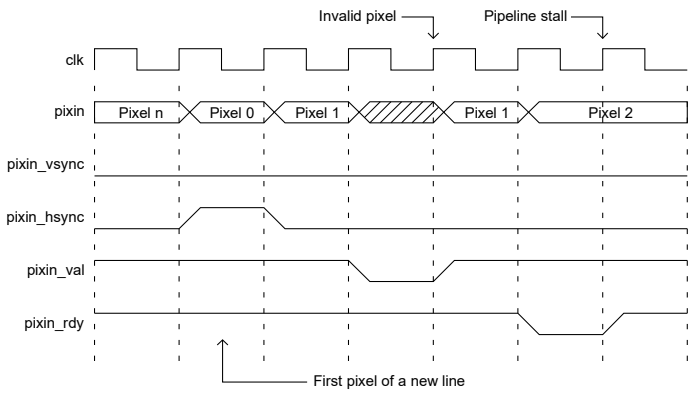


Figure 5: First input pixel of a line

3 Please refer to Zipcores application note: app_note_zc001.pdf for a more detailed explanation of the valid-ready pipeline protocol.

Output video timing

Figures 6 and 7 show the video timing waveforms for a complete frame and a complete line respectively. The position of the active video and the length and duration of the syncs is fully customizable depending on the programmed timing parameters.

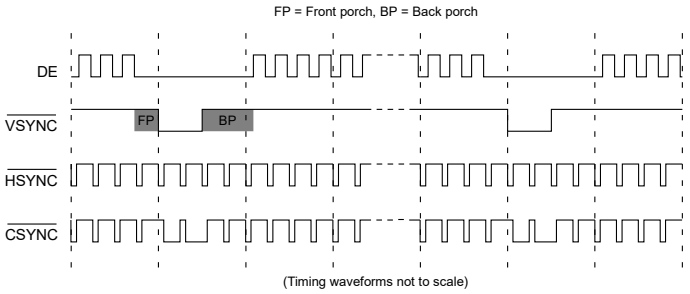


Figure 6: Output video timing (FRAME)

Note that for interlaced video formats, then the vertical timing parameters are different for each field. In this case, the output timing waveforms will be as per Figure 6, but with different FP, BP and SYNC timings for each *field*.

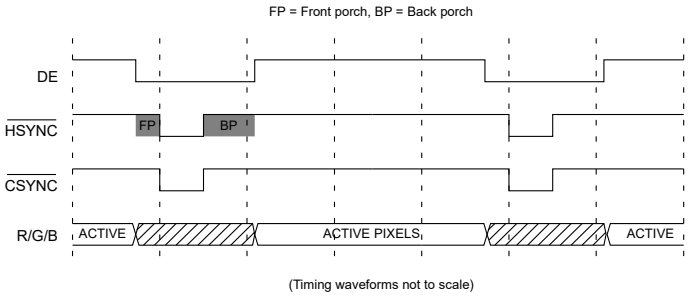


Figure 7: Output video timing (LINE)

Source File Description

All source files are provided as text files coded in VHDL. The following table gives a brief description of each file.

Source file	*Description*
video_file_reader.vhd	Video source file reader
vid_timing_fifo.vhd	Asynchronous pixel FIFO
vid_timing_sof.vhd	Start of frame sync module
vid_timing_cont.vhd	Video timing controller
vid_timing_gen.vhd	Top-level component
vid_timing_gen_bench.vhd	Top-level test bench

Functional Testing

An example VHDL testbench is provided for use in a suitable VHDL simulator. The compilation order of the source code is as follows:

1. video_file_reader.vhd
2. vid_timing_fifo.vhd
3. vid_timing_sof.vhd
4. vid_timing_cont.vhd
5. vid_timing_gen.vhd
6. vid_timing_bench.vhd

The VHDL test bench instantiates the VID_TIMING_GEN component and the user may modify the timing parameters as required. In the example provided, the test is configured to give an industry standard VGA output display at 640x480 resolution and a 60Hz refresh rate.

The simulation must be run for at least 100 ms during which time the output syncs and RGB output pixels are captured in the file *video_out.txt*.

The output text file follows a simple format which defines the state of signals: *vid_vsync_n*, *vid_hsync_n*, *vid_r*, *vid_g* and *vid_b* on a clock-by-clock basis. The simulation output is shown in Figure 8.

Figure 8: VGA simulation output showing regions of video blanking

Synthesis and Implementation

The files required for synthesis and the design hierarchy is shown below:

- vid_timing_gen.vhd
  - vid_timing_cont.vhd
  - vid_timing_fifo.vhd
  - vid_timing_sof.vhd

The VHDL core is designed to be technology independent. However, as a benchmark, synthesis results have been provided for the Xilinx® 7-series FPGAs. Synthesis results for other FPGAs and technologies can be provided on request.

Fixing the timing parameters at the input will result in the most optimum design and will result in significant area savings. Trial synthesis results are shown below. The design was synthesized with the pixel width *dw* = 8.

Resource usage is specified after Place and Route.

XILINX® 7-SERIES FPGAS

Resource type	***Artix-7***	***Kintex-7***	***Virtex-7***
Slice Register	319	319	320
Slice LUTs	456	444	448
Block RAM	0	0	0
DSP48	0	0	0
Occupied Slices	140	130	132
Clock freq. (approx)	300 MHz	350 MHz	400 MHz

Revision History

Revision	***Change description***	***Date***
1.0	Initial revision	14/12/2009
1.1	Revised the reset scheme. New data enable signal. Added section on video signal output timing.	16/04/2011
1.2	Removed the resync_sof signal. Now using system reset instead. Updated synthesis results in line with new source code.	05/12/2011
1.3	Moved generic timing parameters to ports. Increased internal counters to 16-bit throughout. Updated synthesis results.	15/07/2014
1.4	Added support for interlaced video. Added new separate blanking signals.	27/02/2017
1.5	Moved interlacing control parameters to the ports.	22/01/2019

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