SAP5S / SAP51

Universal Actuator-Sensor Interface IC

Datasheet Revision C

Features

- Universal application in AS-i Slave, Master, Repeater and Bus-Monitor components
- Support of AS-i Complete Specification V3.0, including all optional features
  - Synchronous Data I/O Mode
  - 4 Input / 4 Output operation in Extended Address Mode
  - User write protection for Extended ID-Code 1
  - Multiplexed Parameter Port
- Full support of the AS-i “Safety at Work” concept
- On chip electronic inductor with current drive capability of 55mA
- LED outputs supporting all status indication modes defined by AS-i Complete Specification V3.0
- Data preprocessing functions: input filtering and input inverting
- Support of 5.33 / 16 MHz crystals by automatic frequency detection
- Clock Watchdog for high System Security
- Communication Watchdog

Description

SAP5 is a monolithic CMOS integrated circuit certified for AS-i (Actuator Sensor Interface) networks. AS-i networks are used for industrial automation.

AS-i is designed for easy and simple interconnection of binary sensors and actuators. It uses a two-wire unshielded cable to transport power and information.

Using the SAP5 safety-related AS-i slaves can be realized according to the AS-i “Safety at Work” concept. Slaves complying with category 4 of EN954-1 can be realized with a minimum of external circuitry.

The device is available in SOP20 and SOP16 package.

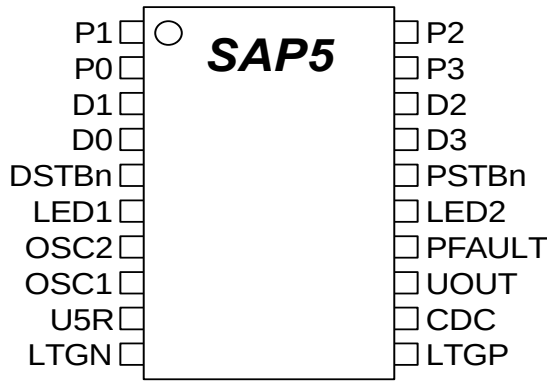
Application Support

Configuration of the chip is handled through programming of the on-chip E²PROM. ZMD provides special tools to ease product evaluation and selection of different operation modes.

AS-Interface Programmer 2.0 USB
(Ordering Code: 3600100145)

SAP5 Evaluation Board 2.0
(Ordering Code: 3600100144)

Further application support is available through e-mail hotline under asi@zmd.de



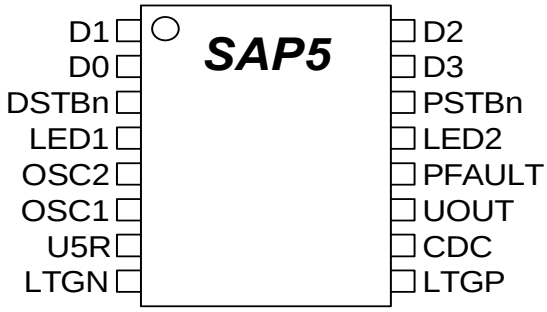


Table of Contents

Page

0 Read this First

0.1 Important Notice

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ZMD reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

0.2 References

[1] AS-Interface Complete Specification Version 3.0, dated 16.09.2004

[2] Spezifikation der sicheren AS-i-Übertragung, Leuze electronic, 12.05.2000

0.3 Revision History

Revision	Date	Technical Changes	Page in Datasheet
B	September 2005	First marketed silicon version	
C	March 2007	Modified I_{IL} – current range for input low level	Table 16 at Page 25
C	March 2007	Modified Delay Mode activation through parameter port P1	Page 29
C	March 2007	Modified Synchronous Data I/O Mode activation through parameter port P2	Page 30
C	March 2007	Modified Watchdog activation through parameter port P0	Page 40
C	March 2007	Improved Burst protection filter and improved ESD behavior	

1 General Device Specification

1.1 Absolute Maximum Ratings (Non Operating)

Table 1: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
V_{LTGN}	Voltage reference	0	0	V	
$V_{LTGP-LTGN}$	Voltage difference between LTGP and LTGN (V_{LTGP} - V_{LTGN})	0	40	V	1
$V_{LTGP-LTGN\_P}$	Pulse voltage between LTGP and LTGN (V_{LTGP} - V_{LTGN})	0	50	V	2
$V_{inputs1}$	Voltage at pin CDC, D0…D3, P0…P3, DSTBn, PSTBnBn, LED1, LED2, PFAULT, UOUT	-0.3	V_{UOUT}+ 0.3	V	
$V_{inputs2}$	Voltage at pins OSC1, OSC2, U5R	-0.3	7	V	
I_{in}	Input current into any pin except supply pins	-50	50	mA	4
H	Humidity non-condensing				5
V_{HBM}	Electrostatic discharge – Human Body Model (HBM2)	1500		V	6
V_{EDM}	Electrostatic discharge – Equipment Discharge Model (EDM)	200		V	7
θ_{STG}	Storage temperature	-55	125	°C	
θ_{lead}	Soldering temperature Sn/Pb	JEDEC-J-STD-020C 240		°C	
θ_{lead}	Soldering temperature 100%Sn	JEDEC-J-STD-020C 260		°C	
R_{thj-16}	Thermal resistance of SOIC 16 package	80	100	K/W	8
R_{thj-20}	Thermal resistance of SOIC 20 package	75	95	K/W	8

1 reverse polarity protection has to be performed externally,

2 pulse with ≤ 50µs, repetition rate ≤ 0.5 Hz

3 $V_{LTGP-LTGN}$ and $V_{LTGP-LTGN\_P}$ must not be violated

4 Latch-up resistance, reference pin is 0V

5 Level 4 according to JEDEC-020A is guaranteed

6 HBM: C = 100pF charged to V_{HBM2} with resistor R = 1.5kΩ in series, valid for all pins except LTGP-LTGN

7 EDM: C = 200pF charged to V_{EDM} with no resistor in series, valid for LTGP-LTGN only

8 Single layer board, P_{tot} = 0.5W; air velocity = 0m/s ⇒ max. value; air velocity = 2.5m/s ⇒ min. value

1.2 Operating Conditions

Table 2: Operating Conditions

Symbol	Parameter	Min	Max.	Unit	Note
V_{LTGN}	Negative supply voltage	0	0	V	
V_{LTGP}	DC voltage at LTGP relating to V_{LTGN}	16	34	V	1, 2
I_{LTGP}	Operating current at V_{UIN} = 30V		6	mA	3
I_{CL1}	Max. output sink current at pins D3...D0, DSTBn		10	mA	
I_{CL2}	Max. output sink current at pins P0...P3, PSTBnBn		10	mA	
θ_{amb}	Ambient temperature range, operating range	-25	85	°C	

[1] Below $V_{LTGPmin}$ the power supply block may not be able to provide the specified output currents at UOUT and U5R.

[2] Outside of these limits the send current shape and send current amplitude cannot be guaranteed.

[3] f_c = 16.000 MHz, no load at any pin, transmitter turned off, digital state machine is in idle state

Table 3: Crystal Frequency

Symbol	Parameter	Nom.	Unit	Note
f_c	Crystal frequency	5.333/16.000	MHz	4

[4] The IC automatically detects whether the crystal frequency is 5.333MHz or 16.000MHz and controls the internal clock circuit accordingly.

1.3 EMC Behavior

The IC has to fulfill the requirements defined in AS-Interface Complete Specification V2.11 [1] and related test requirements AS-Interface Slave ICs.

In addition to the AS-Interface Complete Specification and in combination with a reference component circuit the IC has to achieve a communication failure rate less than 10% of the allowed failure rate according to the "Fast Transient" test method specified in the related AS-Interface association test procedures.

The above specified behavior is correct by design and has to be proven while IC characterization.

1.4 Quality Standards

The quality of the IC will be ensured according to the ZMD quality standards. ZMD is a qualified supplier according to ISO/TS 16949:2002 and ISO 14001:1996.

The following reference documents apply for the development process:

- Management Regulation: 0410 Product Development procedure
- Process Specification: ZMD C7D 0.6µm Technology

Functional device parameters are valid for device operating conditions specified in chapter 1.2 at page 4. Production device tests are performed within the recommended ranges of V_{LTGP} - V_{LTGN}, θamb = + 25°C (+ 85°C and - 25°C on sample base only) unless otherwise stated.

1.5 Failure Rate

Symbol	Parameter	Max.	Unit
AQL	Acceptance Quality Level	0.1	%
F55	Failure Rate at 55°C	18	FIT
F70	Failure Rate at 70°C	60	FIT
F85	Failure Rate at 85°C	150	FIT
F125	Failure Rate at 125°C	1400	FIT

1.6 Humidity Class

Level 4 according to JEDEC-020A is guaranteed.

1.7 Package Pin Assignment

Table 4: SAP5 Pin List

SOIC 20 Pin #	SOIC 16 pin #	Name	Direction	Type	Description
1	-	P1	I/O	Pull-up/ Open Drain (*)	Parameter port P1 / Data input port 1 at IO-config = 7
2	-	P0	I/O	Pull-up/ Open Drain (*)	Parameter port P0 / Data input port 0 at IO-config = 7
3	1	D1	I/O	Pull-up/ Open Drain	Data port D2
4	2	D0	I/O	Pull-up/ Open Drain	Data port D0
5	3	DSTBn	I/O	Pull-up/ Open Drain	Data Strobe output / Reset input
6	4	LED1	OUT	Open Drain	LED 1 Status Indication
7	5	OSC2	OUT	Analog (5V)	Crystal oscillator
8	6	OSC1	IN	Analog/ CMOS	Crystal oscillator / External clock input
9	7	U5R	OUT	Analog	Regulated 5V power supply
10	8	LTGN	IN	Analog/Supply	AS-i Transmitter/Receiver output, to be connected to AS-i-
11	9	LTGP	IN	Analog/Supply	AS-i Transmitter/Receiver input, to be connected to AS-i+ via reverse polarity protection diode
12	10	CDC	OUT	Analog	external buffer capacitor
13	11	UOUT	OUT	Analog	decoupled actuator/sensor power supply
14	12	PFAULT	IN	Pull-up	Periphery Fault input (LOW = Periphery Fault)
15	13	LED2	OUT	Open Drain	LED 2 status indication
16	14	PSTBnBn	I/O	Pull-up/ Open Drain	Parameter Strobe output
17	15	D3	I/O	Pull-up/ Open Drain	Data port D3
18	16	D2	I/O	Pull-up/ Open Drain	Data port D2
19	-	P3	I/O	Pull-up/ Open Drain (*)	Parameter port P3 / Data input port 3 at IO-config = 7
20	-	P2	I/O	Pull-up/ Open Drain (*)	Parameter port P2 / Data input port 2 at IO-config = 7

All open drain outputs are NMOS based. Pull-up properties at input stages are achieved by current sources referring to U5R.

(*) The pull-up current source on these parameter ports is switched off if the slave device is programmed with I/O configuration code 7 and a *DEXG* master call is processed.

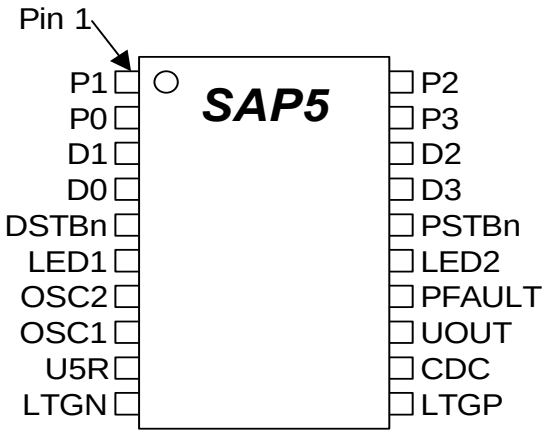


Figure 1: SAP5 Package Pin Assignment for the 20 pin version

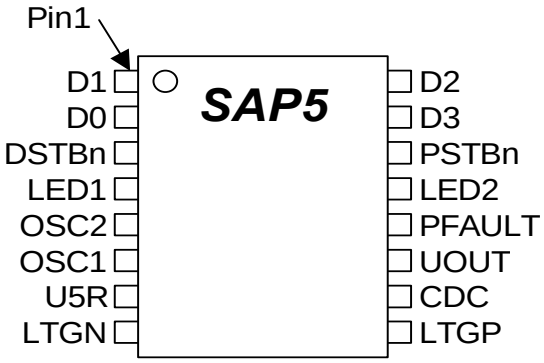


Figure 2: SAP5 Package Pin Assignment for the 16 pin version

2 Basic Functional Description

2.1 Functional Block Diagram

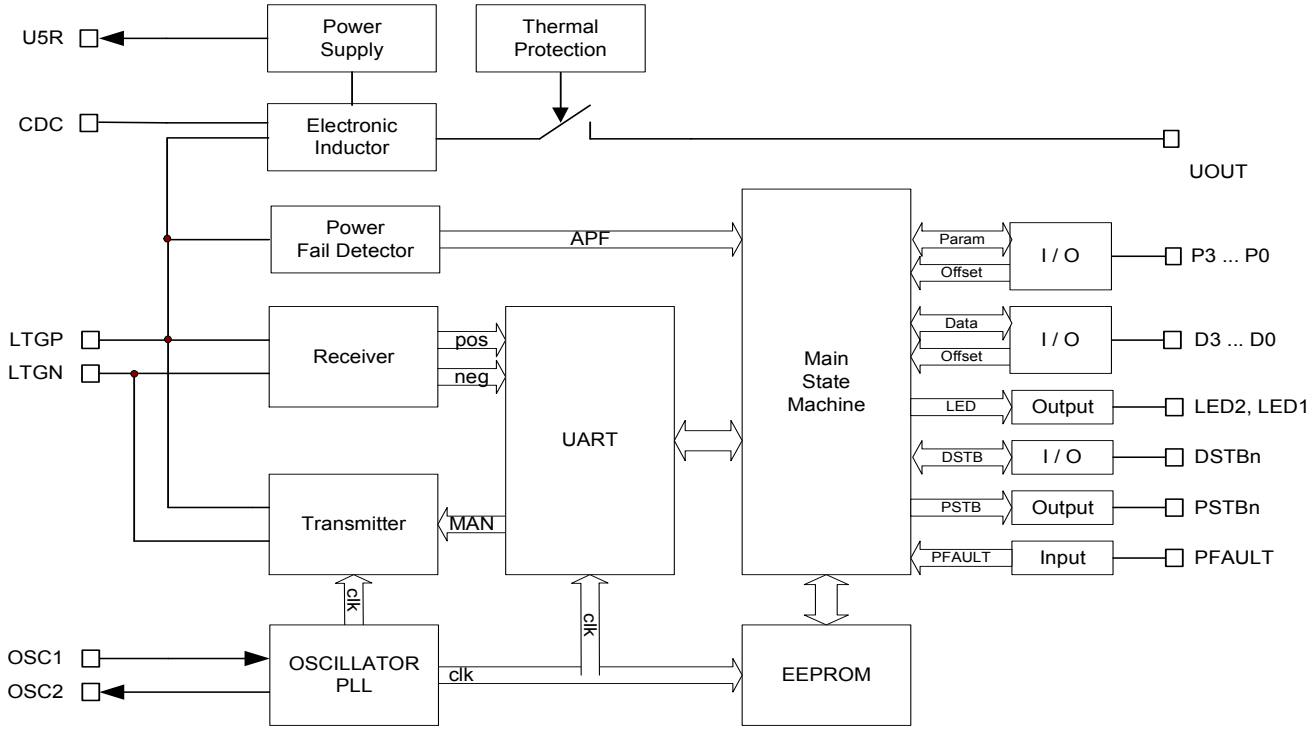


Figure 3: Functional Block Diagram

Following device functions are associated with the different blocks of the IC:

RECEIVER The receive block converts the analog telegram waveform from the AS-i bus to a digital pulse coded signal that can be processed further by a digital UART circuit.

The RECEIVE block is directly connected to the AS-i line pins LTGP and LTGN. It converts the differential AS-i telegram to a single ended signal and removes the DC offset by high pass filtering. To adapt quickly on changing signal amplitudes in telegrams from different network users, the amplitude of the first telegram pulse is measured by a 3 bit flash ADC and the threshold of a positive and a negative comparator is set accordingly to about 50% of the measured level. The comparators generate the P-Pulse and N-Pulse signals.

TRANSMITTER The transmit block transforms a digital response signal to a correctly shaped send current signal which is applied to the AS-i bus. Due to the inductive network behavior of the network the changing send current induces voltage pulses on the network line that overlay the DC operating voltage. The voltage pulses shall have sin²-wave shapes. Hence, the send current shape must follow the integral of the sin²-wave function.

UART / MAIN STATE MACHINE / EEPROM

E²PROM write access and other I/O operations of the Main State Machine are supported in Slave Mode only (see description of general IC operational modes below). In Master Mode the IC is basically equivalent to a physical layer transceiver.

If Slave Mode is activated, the UART demodulates the received telegrams, verifies telegram syntax and timing and controls a register interface to the Main State Machine. After reception of a correct telegram, the UART generates appropriate Receive Strobe signals, that tell the Main State Machine to start further processing. The Main State Machine decodes the telegram information and starts respective I/O processes or E²PROM access. A second register interface is used to send data back to the UART for construction of a telegram response. The UART modulates the response data into a Manchester-II-coded bit stream that is used to control the TRANSMITTER unit.

ELECTRONIC INDUCTOR

The electronic inductor is basically a gyrator circuit. It provides an inductive behavior between the IC pins LTGP and UOUT while the inductance is controlled by the capacitor on pin CDC. The inductor decouples the power regulator of the IC as well as the external load circuit from the AS-i bus and hence prevent cross talk or switching noise from disturbing the telegram communication on the bus.

The AS-i Complete Specification describes the input impedance behavior of a slave module by an equivalent circuit that consists of R, L and C in parallel. For example, a slave module in Extended Address Mode shall have R > 13.5 kOhm, L > 13.5 mH and C < 50pF. The electronic inductor of the SAP5 delivers values that are well within the required ranges for output currents up to 55mA (Uin>24V). More detailed parameters can be found in chapter 4.1.

The electronic inductor requires an external capacitor of 10µF at pin UOUT for stability.

POWER SUPPLY

The power supply block consists of a bandgap referenced 5V-regulator as well as other reverence voltage and bias current generators for internal use. The 5V regulator requires an external capacitor at pin U5R of at least 100nF for stability. It can source up to 4mA for external use, however the power dissipation and the resulting device heating become a major concern, if too much current is drawn from the regulator. See chapter 4.1.

OSCILLATOR / PLL

The oscillator supports direct connection of 5.33 MHz or 16.000 MHz crystals with a dedicated load capacity of 12pF and parasitic pin capacities of up to 8pF. The IC automatically detects the oscillation frequency of the connected crystal and controls the internal clock generator circuit accordingly.

After power-on reset the IC is set to 16.000 MHz operation by default. After about 200µs it will either switch to 5.333 MHz operation or remain in the 16.000 MHz mode. The frequency detection is active until the first AS-i telegram was successfully received in order to make sure the IC found the correct clock frequency setting. The detection result is locked thereafter to increase resistance against burst or other interferences.

The oscillator unit also contains a clock watch dog circuit that can generate an unconditioned IC reset if there was no clock oscillation for more than about 20µs. This is to prevent the IC from unpredicted behavior if no clock signal is available anymore.

THERMAL PROTECTION

The IC is self protected against thermal overload. If the silicon die temperature rises above around 140°C for more than 2 seconds, the IC detects thermal overheating, switches off the electronic inductor, performs an IC reset and sets all analog blocks to power down mode. The 5V-regulator is of course also turned off in this state, however, there will still remain a voltage of about 3 … 3.5V available at U5R that is derived from the internal start circuitry. If the overheat condition is left the IC resumes operation and performs an initialization.

POWER FAIL DETECTOR

The Power Fail Detector observes the voltage at the AS-i-line. It signals at pin PSTBn/APF when the voltage drops below about 22.5V. Active in Master Mode only.

INPUT STAGE

All digital inputs, except of the oscillator pins, have high voltage capabilities and pull-up features. For more details see chapters 1.7, 4.3, 4.7, and 4.8.

OUTPUT STAGE

All digital output stages, except of the oscillator pins, have high voltage capabilities and are implemented as NMOS open drain buffers. Each pin can sink up to 10mA of current. See chapter 4.4.

2.2 General Operational Modes

The SAP5 provides two operational modes: Slave Mode and Master/Repeater Mode. A definition of which operational mode becomes active is made by programming the flag *Master_Mode* in the Firmware Area of the E²PROM (see also Table 9 on page 19). The E²PROM is read out at every initialization of the IC. Online mode switching is not provided. The following configurations apply:

Table 5: Assignment of operational modes

Selected Operational Mode	Master Mode Flag
Slave Mode	0
Master/Repeater Mode	1

In Slave Mode the SAP5 operates as fully featured AS-i Slave IC according to AS-i Complete Specification v3.0.

In Master/Repeater Mode the SAP5 it acts as physical layer transceiver. It translates a digital output signal from the master control logic (etc. PLC, µP, …) to a correctly shaped, analog AS-i pulse sequence and vice versa. Every AS-i telegram received is checked for consistency with the AS-i communication protocol specifications and if no errors were found, an appropriate receive strobe signal is generated.

The following figure shows the different data path configurations.

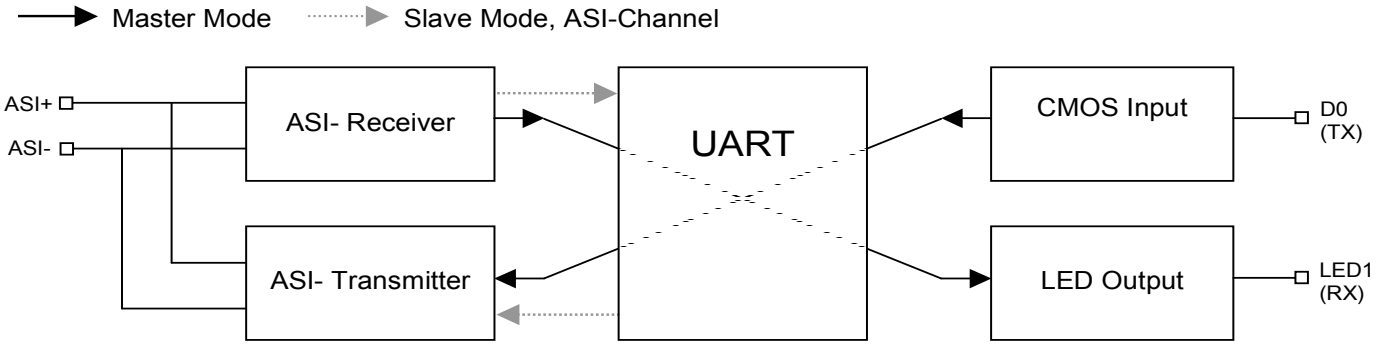


Figure 4: Data path in Master-, Repeater- and Monitor-Mode

More detailed signal descriptions can be found in chapters 4.19 Master- and Repeater Mode as well as 4.14 UART.

2.3 Slave Mode

The Slave Mode is the most complex operational mode of the IC. The SAP5 does not only support all mandatory AS-i Slave functions but also a variety of additional features that eases the design of AS-i Slave modules.

2.3.1 AS-i communication channel

The AS-i channel is directly connected to AS-i Bus via the pins LTGP and LTGN. A receiver and a transmitter unit are connected in parallel to the pins that allow fully bi-directional communication through LTGP and LTGN.

2.3.2 Parameter Port Pins

In the 20-pin package the SAP5 features a 4-bit wide parameter port and a related parameter strobe signal pin PSTBn. AS-i Complete Specification V3.0 newly defines a bidirectional mode for parameter data. The SAP5 supports this feature, that can be activated by special E²PROM setting (*IO_Code*, see chapter 4.9).

There is a defined phase relation between a parameter output event, the parameter input sampling and the activation of the PSTBn signal. Thus it can be used to trigger external logic or a micro controller to process the received parameter data or to provide new input data for the AS-i slave response.

See chapter 4.7 for further details.

2.3.3 Data Port Pins

The SAP5 provides a 4-bit wide data port. The outputs work independently from each other allowing a maximum of 4 output devices to be connected to the SAP5. The direction of the Data Port pins are set through the *IO_Code*, see chapter 4.9.

The data port is accompanied by the data strobe signal DSTBn. There is a defined phase relation between a data output event, the input data sampling and the activation of the DSTBn signal. Thus, it can be used to trigger external logic or a micro controller to process the received data or to provide new input data for the AS-i slave response. See chapter 4.8 for further details.

2.3.4 Data Input Inversion

By default the logic signal (HIGH / LOW) that is present at the data input pins during the input sampling phase is transferred without modification to the send register, which is interfaced by the UART. By that, the signal becomes directly part of the slave response.

Some applications work with inverted logic levels. To avoid additional external inverters, the input signal can be inverted by the SAP5 before transferring it to the send register. The inversion of the input signals can be done jointly for all data input pins. See chapter 4.8.

2.3.5 Data Input Filtering

To prevent input signal bouncing from being transferred to the AS-i Master, the data input signals can be digitally filtered. Activation of the filter is done jointly either by E²PROM configuration or by the logic state of parameter port pin P2. For more detailed information refer to chapter 4.8.

2.3.6 Synchronous Data I/O Mode

AS-i Complete Specification V3.0 newly defines a synchronous data I/O feature, that allows a number of slaves in the network to switch their outputs at the same time and to have their inputs sampled simultaneously. This feature is especially useful if more than 4-bit wide data is to be provided synchronously to an application.

The synchronization point was defined to the data exchange event of the slave with the lowest address in the network. This definition relies on the cyclical slave polling with increasing slave addresses per cycle that is one of the basic communication principles of AS-i. The IC always monitors the data communication and detects the change from a higher to a lower slave address. If such a change was recognized, the IC assumes that the slave with the lower address has the lowest address in the network.

There are some special procedures that become active during the start of synchronous I/O mode operation and if more than three consecutive telegrams were sent to the same slave address. This is described in more detail in chapter *4.8.3*.

2.3.7 4 Input / 4 Output processing in Extended Address Mode

A new feature of AS-i Complete Specification v3.0 is also support of 4-bit wide output data in Extended Address Mode. In Extended Address Mode it was, up to Complete Specification v2.11, only possible to send three data output bits from the master to the slave because telegram bit I3 is used to select between A- and B- slave type for extended slave addressing (up to 62 slaves per network). In normal address mode I3 carries output data for pin D3.

The new definition introduces a multiplexed data transfer, so that all 4-bits of the data output port can be used again. A first AS-i cycle transfers the data for a 2-bit output nibble only, while the second AS-i cycle transfers the data for the contrary 2-bit nibble. Nibble selection is done by the remaining third bit. To ensure continuous alternation of bit information I2 and thus continued data transfer to both nibbles, a special watchdog was implemented that observes the state of I2 bit. The watchdog can be activated or deactivated by E²RPOM setting. It provides a watchdog filter time of about 327ms.

The multiplexed transfer of course increases the refresh time per output by a factor of two, however, some applications can tolerate this increase for the benefit of less external circuitry and better slave address efficiency. The sampling cycle of the data inputs remains unchanged since the meaning of I3 bit was not changed in the slave response with the definition of the Extended Address Mode.

More detailed information is described in chapter *4.8.4*.

2.3.8 AS-i Safety Mode

Using the SAP5 Safety Mode makes it easy to implement a safety-related AS-i slave according to the AS-i Safety at Work concept. Slaves complying with the control category 4 according to EN 954 –1 can be implemented even with a minimum of external circuitry.

In Safety Mode the respond of the SAP5 IC on a *Data_Exchange* master call (*DEXG*) is different. Instead of responding the regular input data provided at the data ports, a 4-bit data word from a specific 8*4 bit code table is transmitted to the master. Cycling the code table is used to transmit another data word with each *DEXG* master call. The data transmission is supervised by a Safety Monitor.

In Safety Mode the use of the enhanced data input features described above is disabled. In this case the safety mode related inputs act as 3-level inputs. See chapter 4.18 for further details.

2.3.9 Enhanced LED Status Indication

The SAP5 IC supports status indication by two LED outputs. More detailed information on the signaling scheme can be found in chapter 4.11.

2.3.10 Communication Monitor/Watchdog

Data and Parameter communication are continuously observed by a communication monitor. If neither *Data_Exchange* nor *Write_Parameter* calls were addressed to and received by the IC within a time frame of about 41ms, a so called No Data/Parameter Exchange status is detected and signaled at LED1.

If the respective flags are set in the E²PROM the communication monitor can also act as communication watchdog, that initiates a complete IC reset after expiring of the watchdog timer. The watchdog mode can also be activated and deactivated by a signal at parameter port pin P0. For more detailed information see chapter 4.17.

2.3.11 Write protection of ID_Code_Extension_1

As defined in AS-i Complete Specification v3.0 the SAP5 also supports write protection for *ID_Code_Extension_1*. The feature allows the activation of new manufacturer protected slave profiles and is enabled by E²PROM setting. It is described in more detail in chapter 4.20.

2.3.12 Summary of Master Calls

In Table 6 and Table 7 on the following pages show the complete set of master calls that are decoded by the SAP5 in Slave Mode. The master calls in Table 7 are intended for programming of the IC by the slave manufacturer only. They become deactivated as soon as the *Lock_EE_PRG* and *Safety_Program_Mode_Disable* flag are set in the Firmware Area of the E²PROM.

AS-i Complete Specification compliance note:

In order to achieve full compliance to the AS-i Complete Specification, the *Program_Mode_Disable* flag must be set by the manufacturer of AS-i slave modules during the final manufacturing and configuration process and before an AS-i slave device is delivered to field application users.

Table 6: SAP5 Master Calls and Related Slave Responses

		Master Request																Slave
Instruction	**MNE**	**ST**	**CB**	**A4**	**A3**	**A2**	**A1**	**A0**	**I4**	**I3**	**I2**	**I1**	**I0**	**PB**	**EB**	**SB**	**I3**	**I2**
Data Exchange	DEXG	0	0	A4	A3	A2	A1	A0	0	D3 ~Sel	D2	D1	D0	PB	1	0	D3	D2
Write Parameter	WPAR	0	0	A4	A3	A2	A1	A0	1	P3 ~Sel	P2	P1	P0	PB	1	0	P3	P2
Address Assignment	ADRA	0	0	0	0	0	0	0	A4	A3	A2	A1	A0	PB	1	0	0	1
Write Extented ID Code_1	WID1	0	1	0	0	0	0	0	0	ID3	ID2	ID1	ID0	PB	1	0	0	0
Delete Address	DELA	0	1	A4	A3	A2	A1	A0	0	0 Sel	0	0	0	PB	1	0	0	0
Reset Slave	RES	0	1	A4	A3	A2	A1	A0	1	1 ~Sel	1	0	0	PB	1	0	0	1
Read IO Configuration	RDIO	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	0	0	PB	1	0	IO3	IO2
Read ID Code	RDID	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	0	1	PB	1	0	ID3	ID2
Read ID Code_1	RID1	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	1	0	PB	1	0	ID3	ID2
Read ID Code_2	RID2	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	1	1	PB	1	0	ID3	ID2
Read Status	RDST	0	1	A4	A3	A2	A1	A0	1	1 ~Sel	1	1	0	PB	1	0	S3	S2
Broadcast (Reset)	BR01	0	1	1	1	1	1	1	1	0	1	0	1	1	1	--- no slave res		

NOTE: In extended address mode the "Select Bit" defines whether the A-Slave or B-Slave is being addressed. Dependent on the type
the select bit information (Sel) or the inverted select bit information (~Sel). The extended address mode can **not** be activated, a
Lock_EE_PRG is at logic LOW level. Refer to chapter 3.3 on page 20 for programming the *Lock_EE_PRG* flag.

Table 7: SAP5 Additional Master Calls for Slave Configuration

		Master Request															Slave	
Instruction	**MNE**	**ST**	**CB**	**A4**	**A3**	**A2**	**A1**	**A0**	**I4**	**I3**	**I2**	**I1**	**I0**	**PB**	**EB**	**SB**	**I3**	**I2**
Set ID Code	(RDIO)	0	1	A4	A3	A2	A1	A0	1	1	0	0	0	PB	1	0	0	1
Set IO Config	(RDID)	0	1	A4	A3	A2	A1	A0	1	1	0	0	1	PB	1	0	0	1
Set ID Code 2	(RID1)	0	1	A4	A3	A2	A1	A0	1	1	0	1	0	PB	1	0	0	1
Set Control Code	(RID2)	0	1	A4	A3	A2	A1	A0	1	1	0	1	1	PB	1	0	0	1
Set Control Code 2	(RES)	0	1	A4	A3	A2	A1	A0	1	0	1	0	0	PB	1	0	0	1
Enter Program Mode Safety	PRGM	0	1	0	0	0	0	0	1	1	1	0	1	1	1	--- no slave res		

3 E²PROM

3.1 Overview

The SAP5 provides an on-chip E²PROM with typical write and read times according to Table 8.

Table 8: E²PROM Read and Write Times

Symbol	Parameter	Min	Max.	Unit	Note
t_{read_init}	Initialization readout time		50.0	µs	[1]
t_{wrt_adra1}	Write time after *ADRA* master request		38.0	ms	[2]
t_{wrt_adra2}	Write time after *ADRA* master request		12.5	ms	[3]
t_{wrt_wid1u}	Write time after *WID1* master request (user access)		38.0	ms	[2]
t_{wrt_wid1m}	Write time after *WID1* master request (manufacturer access)		25.0	ms	[3]
t_{wrt_prgm}	Single cell write time		12.5	ms	[4]

[1] Time includes readout of the configuration block. Running in Safety Mode, the User/Firmware Area and the Safety Area will be read out in parallel.

[2] the *Lock_EE_PRG* flag is set

[3] the *Lock_EE_PRG* flag is not yet set

[4] concerns the programming of data in both Firmware Area and Safety Area

For security reasons the memory area is structured in three independent data blocks and a single configuration block containing the *Security_Flag*. The data blocks are named User Area, Firmware Area and Safety Area.

The Firmware Area contains all manufacturing related configuration data (i.e. selection of optional features, ID codes, …). It can be protected against undesired data modification by setting the *Lock_EE_PRG* flag to '1'.

The User Area contains only such data that is relevant for changes at the final application (i.e. field installation of slave module). Because the environment where modifications of the user data may become necessary can sometimes be rough and unpredictable, additional security was added to the programming of the User Area, ensuring a write access cannot result in an undetected corruption of E²PROM data.

The Safety Area contains the cryptographic code table for the Safety Mode.

The E²PROM cells in User Area, Firmware Area and Safety Area have a word width of 6 bit. The sixth bit is not shown in Table 9 and Table 11. The sixth bit of each cell represents the odd parity of the respective data word, providing an additional data security mechanism. The programming of the parity bit is performed automatically during the E²PROM write process and cannot be influenced by the user. Each E²PROM read process – particularly during initialization of the SAP5 – involves an evaluation of the parity bits. In case a wrong parity bit was found in the User Area, the entire User Area data is treated as corrupted. The IC returns to Slave Address "0" and the *ID_Code* as well as the *IO_Code* are set to 0xF. In case a false parity bit was found in one or more cells of the Firmware Area or the Safety Area, the status register bit S1 will be set (='1'), signaling the same state as the input PFAULT would be set (refer to chapter 4.16 page 40).

3.2 User Area Programming

User Area data can be written by an *ADRA* or *WID1* master request (refer to Table 6). Any such write access is accompanied by two write steps to the *Security_Flag*, one before and one after the actual modification of user data.

The following procedure is executed when writing to the User Area of the E²PROM:

1. The *Security_Flag* is programmed to '1'.
2. The content of the *Security_Flag* is read back, verifying it was programmed to '1'.
3. The user data is modified.

4. A read back of the written data is performed.
5. If the read back has proven successful programming of the user data, the *Security_Flag* is programmed back to ‘0’.
6. The content of the *Security_Flag* is read back, verifying it was programmed to ‘0’.

Successful execution of the E²PROM write procedure may be observed at the status register contents. If bit S0 is set (logic HIGH) the write process is not finished yet and the programming data is still volatile. If bit S3 (equals the *Security_Flag*) is set, the write procedure did not successfully complete either because the write cycle was interrupted or due to an internal error. In order to program the data correctly the write request should be repeated. The status register can be read using the AS-i Master call *Read_Status* (*RDST*).

In addition to a read out of the data areas, the *Security_Flag* of the E²PROM is also read and evaluated during IC initialization. In case the value of the *Security_Flag* equals ‘1’ (i.e. due to an undesired interruption of a User Area write access), the entire User Area data is treated as corrupted. The IC returns to Slave Address “0” and the *ID_Code* as well as the *IO_Code* are set to 0xF. Consequently, the programming of the User Area data can be repeated.

Table 9: SAP5 E²PROM - User and Firmware Area Content

Internal E²PROM Address	Bit Position	E²PROM Cell Content	Description
0	4 … 0	*A4 … A0*	Slave address
1	2 … 0	*ID1_Bit2 … ID1_Bit0*	*ID_Code_Extension_1* (user configurable)
	3	*ID1_Bit3*	*ID_Code_Extension_1*, A/B slave selection in extended address mode
	4		Not implemented
2	3 … 0	*ID1_Bit3 … ID1_Bit0*	*ID_Code_Extension_1* (manufacturer configurable)
	4		Not implemented
3	4 … 0		Not implemented
4	4	*Synchronous_Data_IO*	Synchronized Data I/O mode
	3 … 0	*ID_Bit3 … ID_Bit0*	*ID_Code*
5	4	*Inhibit_Write_ID1*	*ID_Code_Extension_1* is manufacturer configurable, refer to page 41
	3 … 0	*ID2_Bit3 … ID2_Bit0*	*ID_Code_Extension_2*
6	4	*P1_Delay_Activation*	If flag is set, the logic value at the parameter pin P1 determines whether the *Delay_Mode* function is active or inactive, refer to Table 22
	0 … 3	*IO_Bit3 … IO_Bit0*	*IO_Code*
7	4	*Lock_EE_PRG*	Programming of the E²PROM Firmware region is possible as long as this flag is **not** set (logic LOW).
	3	*Delay_Mode*	activates the *Delay_Mode* function, refer to Table 22
	2	*Invert_Data_In*	All Data Port inputs are inverted.
	1	*Inhibit_BR01*	If flag is set, the master call *BR01* is not executed.
	0	*Inhibit_Watchdog*	If flag is set, the watchdog is **not** activated.
8	4	*P2_Sync_Activation*	The Synchronized Data I/O mode may be activated by Parameter bit P2 as described in Table 23 on page 30.
	3	*Ext_Addr_4I/4O_Mode*	4 Input/ 4 Output Mode in Extended Address Mode
	2	*Parallel_Out_4I/4O*	enables the parallel data output option in Extended Address 4I/4O Mode
	1	*Master_Mode*	Master/Repeater Mode Flag
	0	*P0_Watchdog_Activation*	The watchdog can be enabled/disabled by the logic value at the parameter pin P0.
9	4 … 0	Analogue circuitry trim information	
10			
11			

User Area Firmware Area

3.3 Firmware Area Programming

In order to program one of the 5-bit cells of the Firmware Area (address 4…8) a special master call according to Table 10 must be applied, followed by a *DEXG* or *WPAR* call immediately. Write access to the Firmware Area is possible as long as the *Lock_EE_PRG* flag is not set. The write procedure is started after receipt of the *DEXG*/*WPAR* call. Finish of write procedure may be observed at the status register S0 as described above.

The analogue circuitry trim information (address 9…11) can be written by special test mode operation only.

There is no possibility to read out the E²PROM data directly. However, AS-i-related configuration data like *ID_Code* may be read by the respective *Read_ID_Code* master request.

Table 10: SAP5 E²PROM - User and Firmware Area Programming

Internal E²PROM Address	E²PROM Cell Content	Programming Master Calls	
0	*A4 … A0*	*ADRA* Master Call	
1	*ID1_Bit3 … ID1_Bit0*	*WID1* Master Call	
2	*ID1_Bit3 … ID1_Bit0*		
3	Not implemented		
4	*Synchronous_Data_IO*	I4	Set ID Code (RDIO) [1] + DEXG/WPAR [2]
	ID_Bit3 … ID_Bit0	I3 … I0	
5	*Inhibit_Write_ID1*	I4	Set ID Code 2 (RID1) [1] + DEXG/WPAR [2]
	ID2_Bit3 … ID2_Bit0	I3 … I0	
6	*P1_Delay_Activation*	I4	Set IO Config (RDID) [1] + DEXG/WPAR [2]
	IO_Bit3 … IO_Bit0	I3 … I0	
7	*Lock_EE_PRG*	I4	Set Control Code (RID2) [1] + DEXG/WPAR [2]
	Delay_Mode	I3	
	Invert_Data_In	I2	
	Inhibit_BR01	I1	
	Inhibit_Watchdog	I0	
8	*P2_Sync_Activation*	I4	Set Control Code 2 (RES) [1] + DEXG/WPAR [2]
	Ext_Addr_4I/4O_Mode	I3	
	Parallel_Out_4I/4O	I2	
	Master_Mode	I1	
	P0_Watchdog_Activation	I0	
9	Analogue circuitry trim information	Accessible by ZMD only	
10			
11			

[1] according to Table 7

[2] according to Table 6 with information bits corresponding to the left-hand column; *DEXG* if I4='0', *WPAR* if I4='1'. Note: Differing from regular *WPAR*/*DEXG* calls, the slave always returns the received data bits I3…I0.

☐ User Area ▢ Firmware Area

3.4 Safety Area Programming

The *Safety Area* contains the cryptographic code table which consists of 8 data words and one swap-flag each (refer to chapter 4.18 on page 41 for an explanation of the SAP5 Safety Mode). Similar to the Firmware Area it can be protected against undesired data modification by setting the *Safety_Program_Mode_Disable* flag to '1', see Table 11.

NOTE: Once the *Safety_Program_Mode_Disable* flag is set, the Safety Area of the E²PROM is **permanently** locked, i.e. write access to the *Safety Area* as described in chapter 3.4 is possible only as long as the *Safety_Program_Mode_Disable* is set to *'0'.*

Table 11: SAP5 E²PROM - Safety Area Content

Logical E²PROM Address	Bit Position	E²PROM Cell Content	Description
1	4	*S_flag 0*	swap flag 0
	3 … 0	*DI_S0 3 … 0*	Data Input word 0 from Safety Code Table
2	4	*S_flag 1*	swap flag 1
	3 … 0	*DI_S1 3 … 0*	Data Input word 1 from Safety Code Table
3	4	*S_flag 2*	swap flag 2
	3 … 0	*DI_S2 3 … 0*	Data Input word 2 from Safety Code Table
4	4	*S_flag 3*	swap flag 3
	3 … 0	*DI_S3 3 … 0*	Data Input word 3 from Safety Code Table
5	4	*S_flag 4*	swap flag 4
	3 … 0	*DI_S4 3 … 0*	Data Input word 4 from Safety Code Table
6	4	*S_flag 5*	swap flag 5
	3 … 0	*DI_S5 3 … 0*	Data Input word 5 from Safety Code Table
7	4	*S_flag 6*	swap flag 6
	3 … 0	*DI_S6 3 … 0*	Data Input word 6 from Safety Code Table
8	4	*S_flag 7*	swap flag 7
	3 … 0	*DI_S7 3 … 0*	Data Input word 7 from Safety Code Table
31	1	*Safety_Mode_Enable*	If set, Safety Mode can be enabled
	0	*Safety_Program_Mode_Disable*	If set, Safety Area is protected against overriding

Similar to the Firmware Area programming, Safety Area programming is intended to be used only during production set-up of a slave component at the manufacturer's site. Write Access to the Safety Area of the E²PROM is feasible in the so called Safety Program Mode. It can be entered only if the *Safety_Program_Mode_Disable* flag is not yet set and if the slave address was set to 0x0. In the case that the slave address equals zero, the reception of the *Enter_Program_Mode_Safety* (*PRGM*) call sets the SAP5 device into the Safety Program Mode. It should be noted that no response is generated to the *Enter_Program_Mode_Safety* call (refer to AS-i Complete Specification).

Being in the Safety Program Mode, the *Write_Parameter* (*WPAR*) and *Data_Exchange* (*DEXG*) calls are used to transfer data words to the E²PROM similar to the Firmware Area write procedure described above. However, the address bits A4...A0 of the master telegrams are used to address one of the memory locations of the E²PROM (refer to Table 11). The information bits I4...I0 (normally used for output data) carry the data which shall be stored.

Any *WPAR* or *DEXG* call initializes an autonomous write process within the IC. The status of the write process can be monitored by evaluating the status register of the IC the same way described above. Since the IC is still in Safety Program Mode, the address within the *Read_Status* master call doesn't care. In order to execute as many write procedures as desired, the Safety Program Mode must not be left. However, the SAP5 will leave the Safety Program Mode and start it's initialization procedure if it receives a *Reset_Slave* (*RES*) master call to any desired slave address.

Any attempt to access one of the not available E²PROM address locations (0, 9 … 30) through a *Write_Parameter* (*WPAR*) or *Data_Exchange* (*DEXG*) command will be ignored.

There is no direct read access to the Safety Area data in Safety Program Mode.

An E²PROM verification procedure should be carried out e.g. by performing one complete AS-i safety cycle (8 *DEXG* calls in minimum 250µs intervals) in Safety Mode operation.

4 Detailed Functional Description

4.1 Power Supply

The power supply block provides a sensor supply, which is inductively decoupled from the AS-i bus voltage, at pin UOUT. The decoupling is realized by a Electronic Inductor circuit, which basically consists of a current source and a controlling low pass. The time constant of the low pass that has influence to the resulting input impedance at pin UIN, can be adjusted by an external capacitor at pin CDC.

A second function of the power supply block is to generate a regulated 5V supply for operation of the internal logic and some analog circuitry. The voltage is provided at pin U5R an can be used to supply external circuitry as well, as long as the current requirements stay within in the specified limits (Table 2 at page 6). Because the 5V supply is generated out of the decoupled sensor supply at UOUT, the current drawn at U5R has to be subtracted from the total available load current at UOUT.

The power supply dissipates the major amount of power:

$Ptot = V_{Drop} * (I_{UOUT} + I_{5V}) + (V_{UOUT}-5V) * I_{5V}$

In total, the power dissipation shall not exceed the specified values of chapter 1.1.

To cope with fast internal and external load changes (spikes) external capacitors at UOUT and U5R are required. The LTGN pin defines the ground reference voltage for both UOUT and U5R.

4.1.1 Voltage Output Pins UOUT and U5R

Table 12: Properties of voltage output pins UOUT and U5R

Symbol	Parameter	Min	Max	Unit	Note
V_{UIN}	Positive supply voltage for IC operation	16	34	V	[1]
V_{DROP}	Voltage drop from pin LTGP to pin UOUT	5.2	7.8	V	V_{UIN} > 22V [2]
V_{UOUT}	UOUT output supply voltage	V_{UIN}- $V_{DROPmax}$	V_{UIN}- $V_{DROPmin}$	V	$I_{UOUTmax}$
V_{UOUTp}	UOUT output voltage pulse deviation		1.5	V	[3]
t_{UOUTp}	UOUT output voltage pulse deviation width		2	ms	[3]
V_{U5R}	5V supply voltage	4.75	5.25	V	
I_{UOUT}	UOUT output supply current	0	55	mA	I_{U5R} = 0 Uin>24V
I_{5V}	U5R output supply current	0	4	mA	
I_o	Total output current I_{UOUT} + I_{5V}		60	mA	
C_{BUOUT}	Blocking capacitance at UOUT	10	470	µF	
C_{B5V}	Blocking capacitance at U5R	100		nF	

[1] Parameter copied from Table 2 at page 6

[2] The actual voltage drop increases with increasing load current at Uout

[3] C_{UOUT} = 10µF, output current switches from 0 to $I_{UOUTmax}$ and vice versa

4.1.2 Input Impedance (AS-i bus load)

Table 13: AS-i Bus Load Properties

Symbol	Parameter	Min	Max	Unit	Note
R_{IN1}	Equivalent resistor of the IC	13,5		kΩ	1,2
L_{IN1}	Equivalent inductor of the IC	13,5		mH	1,2
C_{IN1}	Equivalent capacitor of the IC		30	pF	1,2
R_{IN2}	Equivalent resistor of the IC	13,5		kΩ	1,2
L_{IN2}	Equivalent inductor of the IC	12	13,5	mH	1,2
C_{IN2}	Equivalent capacitor of the IC		15 + (L-12mH)*10pF/mH	pF	1,2
C_{Zener}	Parasitic capacitance of the external over-voltage protection diode (Zener diode)		20	pF	1

[1] The equivalent circuit of a slave, which is calculated from the impedance of the IC and the paralleled external over-voltage protection diode (Zener diode), has to satisfy the requirements of the AS-i Complete Specification for Extended Address Mode slaves.

[2] Subtracting the maximum parasitic capacitance of the external over voltage protection diode (20pF) either the triple R_{IN1}, L_{IN1} and C_{IN1} or the triple R_{IN2}, L_{IN2} and C_{IN2} has to be reached by the IC to fulfill the AS-i Complete Specification.

Table 14: CDC pin parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CDC_IN}	Input voltage range	-0.3		V_{U5R}	V	
C_{CDC}	External decoupling capacitor		100		nF	

Note: A decoupling capacitor defines internal low-pass filter time constant; lower values decrease the impedance but improve the turn-on time. Higher values do not improve the impedance but do increase the turn-on time. The turn-on time also depends on the load capacitor at UOUT. After connecting the slave to the power the capacitor is charged with the maximum current I_{UOUT}. The impedance will increase when the voltage allows the analog circuitry to fully operate.

4.2 Thermal Protection

The IC continuously observes its silicon die temperature. If the temperature rises above around 140°C for more than 2 seconds the IC will cut off the UOUT output from the internal voltage reference. Thus the current consumption of the IC will drop down to its operating current (refer to Table 2). In order to prevent an undesired drawing of transmit current the transmitter is also disabled in case the over temperature cut off condition is true.

After over temperature cut off, the output voltage at UOUT will be restored and the IC performs an initialization if the die temperature has cooled down by 10 … 20°C with an additional time delay of 1s.

Table 15: Cut Off Temperature

Symbol	Parameter	Min	Max	Unit	Note
T_{CutOff}	Chip temperature for over temperature cut off	125	160	°C	

4.3 DC Characteristics – Digital Inputs

The following pins contain digital high voltage input stages:

- Input-only pin: **PFAULT**
- I/O pins: **P1, P3, D1, D3, DSTBn, PSTBn [1], LED1 [1]**
- 3-level I/O pins: **P0, P2, D0, D2 [3]**

Table 16: DC Characteristics of digital high voltage input pins

Symbol	Parameter	Min	Max	Unit	Note
V_{OFL}	Voltage range for input "offset_low" level	0	1.0	V	[3,4]
V_{OFH}	Voltage range for input "offset_high" level	1.6	V_{UOUT}	V	[3,4]
V_{IL2}	Voltage range for input "low" level	0	2.5	V	[4]
V_{IH}	Voltage range for input "high" level	3.5	V_{UOUT}	V	
I_{IL}	Current range for input "low" level	-12	-3	µA	V_{IN} = 1V [2]
I_{IH}	Current range for input "high" level	-10	10	µA	$V_0 \geq V_{U5R}$
C_{DL}	Capacitance at pin DSTBn		10	pF	[5]

[1] PSTBn and LED1 are inputs for test purposes only.

[2] The pull-up current is driven by a current source connected to U5R. It stays almost constant for input voltages ranging from 0 to 3.8V.

[3] Pins P0, P2, D0 and D2 are used as 3-level inputs - i.e. inputs with offset detection - in Safety Mode only, configuration beyond depends on the slave profile (refer to Table 26 on page 34)

[4] The 3-level input pads contain independent comparators for the detection of regular input data level and offset. Refer to Figure 12 on page 44 for constraints to the externally applied voltages in Safety Mode.

[5] The internal pull-up current is sufficient to avoid accidental triggering of an IC reset if the DSTBn pin remains unconnected. For external loads at DSTBn a sufficient pull up resistor is required to ensure $V_{IH} \geq 3.5V$ in less than 90ms after the beginning of a DSTBn = Low pulse.

4.4 DC Characteristics – Digital Outputs

The following pins contain digital high voltage open drain output stages:

- Output-only pin: **LED2**
- I/O pins: **D0 … D3, P0 … P3, DSTBn, PSTBn[1], LED1[1]**

Table 17: DC Characteristics of digital high voltage output pins

Symbol	Parameter	Min	Max.	Unit	Note
V_{OL1}	Voltage range for output "low" level	0	1	V	I_{OL1} = 10mA
V_{OL2}	Voltage range for output "low" level	0	0.4	V	I_{OL2} = 2mA
I_{OH}	Output leakage current	-10	10	µA	$V_{0H} \geq V_{U5R}$

[1] PSTBn and LED1 are inputs for test purposes only.

A slew rate limitation is provided to each digital high voltage output driver which limits the rise and fall times for both High/Low and Low/High transitions to 40…50ns.

NOTE: The rise time for a Low/High transition is mainly influenced by the external pull-up resistor.

4.5 AS-i Receiver

The receiver detects (telegram) signals at the AS-i line, converts them to digital pulses and forwards them to the UART for further processing. The receiver is internally connected between the LTGP and LTGN pins.

Functional, the receiver removes the DC value of the input signal, band-pass filters the AC signal and extracts the digital output signals from the $\sin^2$-shaped input pulses by a set of comparators. The amplitude of the first pulse determines the threshold level for all following pulses. This amplitude is digitally filtered to guarantee stable conditions and to suppress burst spikes. This approach combines a fast adaptation to changing signal amplitudes with a high detection safety. The comparators are reset after every detection of a telegram pause at the AS-i line.

When the receiver is turned on, the transmitter is turned off to reduce the power consumption.

Table 18: Receiver Parameters

Symbol	Parameter	Min	Max	Unit	Note
V_{SIG}	AC signal peak-peak amplitude (between LTGP and LTGN)	3	8	V	
V_{LSIGon}	Receiver comparator threshold level (refer to Figure 5)	45	55	%	Related to amplitude of 1st pulse

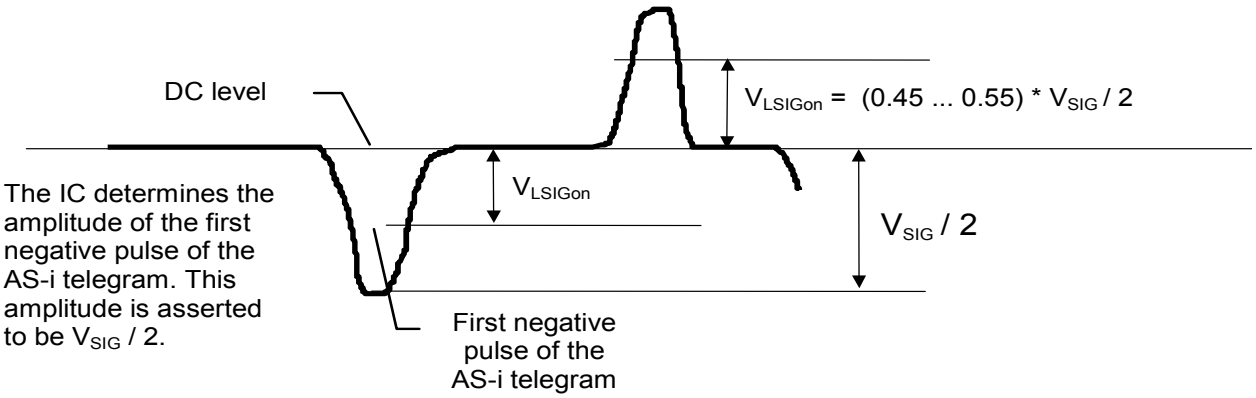


Figure 5: Receiver comparator threshold set-up in principle

4.6 AS-i Transmitter

The transmitter draws a modulated current between LTGP and LTGN to generate the communication signals. The shape of the current corresponds to the integral of a $\sin^2$-function. The transmitter comprises a current DAC and a high current driver. The driver requires a small bias current to flow. The bias current is ramped up slowly a certain time before the transmission starts so that any false voltage pulses on the AS-i line are avoided.

When the transmitter is turned on, the receiver is turned off to reduce the power consumption. The SAP5 comprises a Clock Watchdog that becomes activated once the clock signal is stopped for about 100µs … 150µs. Thus, the transmitter is prevented from being permanently switched on in case the clock signal is missing.

Table 19: Transmitter Current Amplitude

Symbol	Parameter	Min	Max	Unit	Note
I_{SIG}	Modulated transmitter peak current swing (between LTGP and LTGN)	55	68	mA	

4.7 Parameter Port and PSTBn

The parameter port is always configured for continuous bi-directional operation. However, once *IO_Code*=0x7 (see Table 25), the parameter ports will return to high impedance state right after a *WPAR* request because they act as data input ports or safety data ports for a following *DEXG* master call.

Every pin contains an NMOS open drain output driver plus a high voltage high impedance digital input stage. Received parameter output data is stored at the Parameter Output Register and subsequently forwarded to the open drain output drivers. A certain time ($t_{PI\text{-}latch}$) after new output data has arrived at the port, the corresponding inputs are sampled. Due to the open drain character of the output driver, the input value results from a wired AND combination of the parameter output value and such signals driven to the port by external sources.

The availability of new parameter output data is signaled by the Parameter Strobe (PSTBn) signal as shown in Figure 6.

Besides the basic I/O function, the first parameter output event after an IC reset has an additional meaning. It enables the data exchange functionality.

Any IC reset turns the Parameter Output Register to 0xF and forces the parameter output drivers to high impedance state. Simultaneously, a Parameter Strobe is generated, having the same t_{setup} timing and t_{PSTBn} pulse width, as new output data would be driven.

Table 20: Timing Parameter Port

Symbol	Parameter	Min	Max	Unit	Note
t_{STB}	Output data is valid after PSTBn HIGH-LOW edge	0.0	1.5	µs	
t_{PSTBn}	Pulse width of Parameter Strobe (PSTBn)	6.0	6.8	µs	[1]
$t_{PI\text{-}latch}$	Acceptance of input data	10.5	12.5	µs	[2]
$t_{P\text{-}off}$	Parameter Port is at high impedance state after PSTBn HIGH-LOW edge	56.0	64.5	µs	[3]

[1] The timing of the resulting voltage signal also depends on the external pull up resistor.

[2] The parameter input data must be stable within the period defined by min. and max. values of $t_{PI\text{-}latch}$.

[3] concerns the IO configuration “7” only

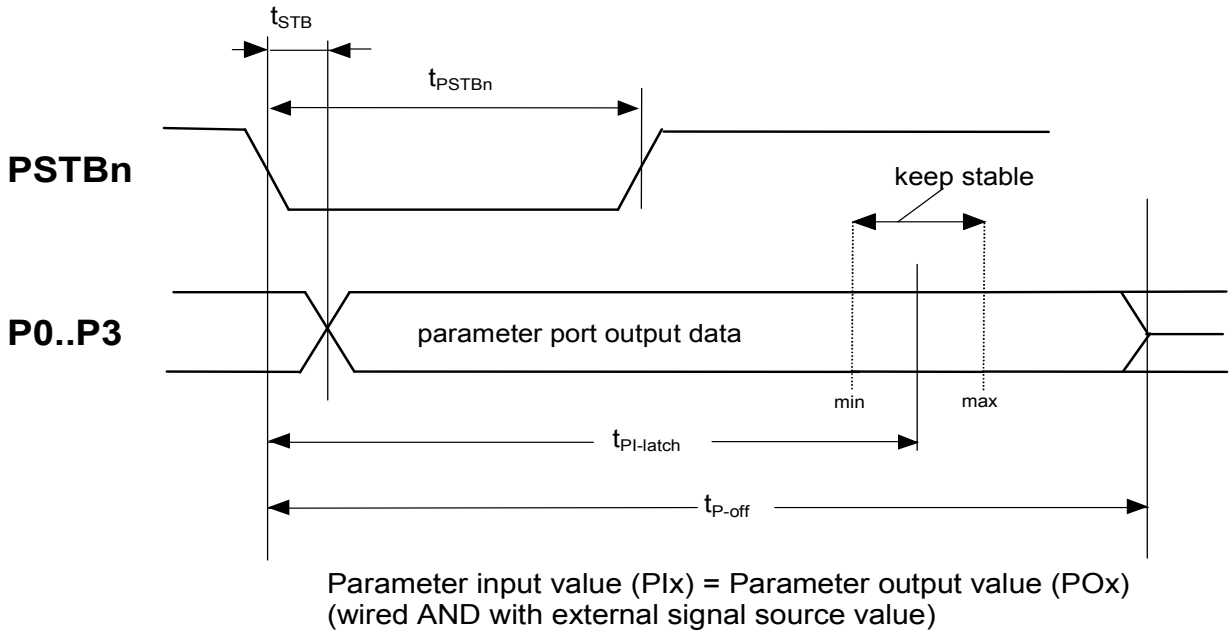


Figure 6: Timing Diagram Parameter Port P0 ... P3, PSTBn

4.8 Data Port and DSTBn

4.8.1 Timing of Data I/O and DSTBn

Every data pin (D0…D3) contains an NMOS open drain output driver as well as a high voltage high impedance input stage. Received output data is stored at the Data Output Register and subsequently forwarded to the data pins. A certain time ($t_{DI\text{-}latch}$) after new output data was written to the port the input data is sampled.

The availability of new output data is signaled by the Data Strobe (DSTBn) signal as shown in Figure 7. The DSTBn pin has an additional reset input function, which is described further in chapter 4.13 IC Reset.

Any IC reset turns the Data Output Register to 0xF and forces the data output drivers to high impedance state. Simultaneously, a Data Strobe is generated, having the same t_{setup} timing and t_{DSTBn} pulse width, as new output data would be driven.

Table 21: Timing Data Port Outputs

Symbol	Parameter	Min	Max	Unit	Note
t_{STB}	Output data is valid after DSTBn HIGH/LOW edge	0.0	1.5	µs	
t_{hold}	Output driver is at high impedance state after DSTBn LOW/HIGH	0.2	1.0	µs	1
t_{DSTBn}	Pulse width of Data Strobe (DSTBn)	6.0	6.8	µs	2
$t_{DI\text{-}latch}$	Acceptance of input data	10.5	12.5	µs	3

[1] Parameter is only valid if the respective data port is configured as I/O pin.

[2] The timing of the resulting voltage signal also depends on the external pull up resistor.

[3] The input data must be stable within the period defined by min. and max. values of $t_{DI\text{-}latch}$.

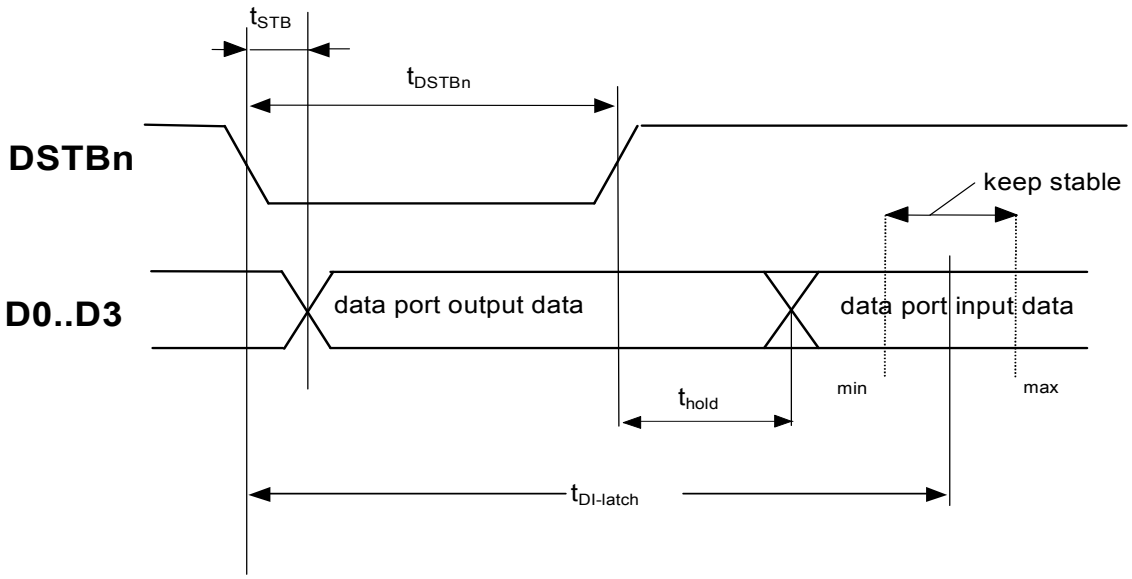


Figure 7: Timing diagram data port D0 ... D3 and DSTBn

4.8.2 Input Data Pre-Processing

Besides the standard input function the Data Port offers different data pre-processing features that can be activated by setting corresponding flags in the Firmware Area of the E²PROM.

- **Input Inverting**

The input values of all four data input channels are inverted if the *Invert_Data_In* flag is set.

- **Input Delay**

If the Delay Mode is activated, a new input value is returned to the master if equal input data was sampled for two consecutive *Data_Exchange* cycles. As long as the condition is not true, previous valid data is returned. To suppress undesired input data validation in case of immediately repeated *Data_Exchange* calls (i. e. AS-i Masters immediately repeat one *Data_Exchange* requests if no valid slave response was received on the first request) input data sampling is blocked for 256µs (-6.25%) after every sampling event.

The filter output of each data port is preset to “0” after reset or as long as the *Data_Exchange_Disable* flag is set, respectively.

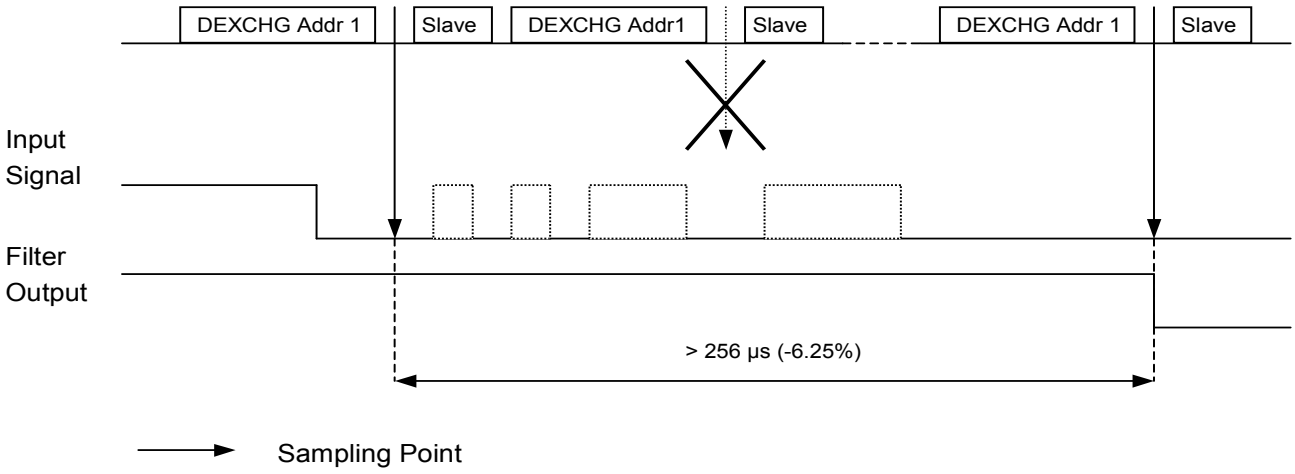


Figure 8: Principle of Delay Mode input filtering (exemplary for Slave with Address 1)

Activation of Delay Mode depends on the E²PROM flags *Delay_Mode* and *P1_Delay_Activation* and the value of the Parameter Port P1 Output Register as shown in Table 22. Delay Mode cannot be activated when Safety Mode is enabled.

Note: The input signal at Parameter Port P1 does not influence activation of **Input Delay Mode** at all. Only the master can change the activation status by sending a corresponding **Write_Parameter** (WPAR) request.

Table 22: Activation of *Delay Mode*

Delay_Mode	*P1_Delay_Activation*	Parameter P1 Output Register	*Delay Mode*
0	X	X	**OFF**
1	0	X	**ON**
1	1	1	**OFF**
1	1	0	**ON**

4.8.3 Synchronous Data I/O Mode

Since the slaves in an AS-i network are called successively by the master, the data input and output operations of different slaves are not synchronized normally. If there is, however, an application that requests accurate synchronized data I/O timing, the respective slaves may be operated in the Synchronous Mode. Concerning the communication with the master, slaves running in the Synchronous Mode behave like regular slaves. However, the input data sampling as well as the output data driving is determined by the polling cycle of the respective AS-i network as described below.

Activation of the SAP5 Synchronous Mode is related to the E²PROM flags *Synchronous_Data_IO* and *P2_Sync_Activation* (refer to Table 9) and the value of the Parameter Port P2 Output Register as follows:

NOTE: The input signal at Parameter Port P2 does not influence activation of **Synchronous Data I/O Mode** at all. Only the master can change the activation status by sending a corresponding **Write_Parameter** (WPAR) request.

Table 23: Activation of *Synchronous Mode*

Synchronous_Data_IO	*P2_Sync_Activation*	Parameter P2 Ouput Register	*Synchronous Mode*
0	X	X	**OFF**
1	0	X	**ON**
1	1	1	**OFF**
1	1	0	**ON**

NOTE: The Synchronous Mode is not available if Safety Mode is enabled.

With activated Synchronous Mode, input data sampling as well as output data driving events are moved to different times **synchronized** to the polling cycle of the AS-i network. Nevertheless, the communication principles between master and slave remain unchanged compared to regular operation. Following rules apply:

- Data I/O is triggered by the *DEXG* call to slave with the lowest slave address in the network. Based on the fact, that a master is calling slaves successively with rising slave addresses, the SAP5 considers the trigger condition true, if the slave address of a received *DEXG* call is less than the slave address of the previous (correctly received) *DEXG* call.

  Data I/O is only triggered, if the slave has (correctly) received data during the last cycle. If the slave did not receive data (i.e. due to a communication error) the Data Outputs are not changed and no Data Strobe is generated (arm+fire principle). The inputs however, are always sampled at the trigger event.
- If **the slave with the lowest address in the network** is operated in the Synchronous Mode, it postpones the output event for the received data for a full AS-i cycle. This is to keep all output data of a particular cycle image together.

  Note: To make this feature useful, the master shall generate a data output cycle image once before the start of every AS-i cycle. The image is derived from the input data of the previous cycle(s) and other control events. Once an AS-i cycle has started, the image shall not change anymore. If A- and B- slaves are installed in parallel at one address, the master shall address all A-Slaves in one cycle and all B-Slaves in the other cycle.

  The input data, sampled at the slave with the lowest slave address in the network, is sent back to the master without any delay. Thus, the input data cycle image is fully captured at the end of an AS-i cycle, just as in networks without any Synchronous Mode slaves. In other words, the input data sampling point has simply moved to the beginning of the AS-i cycle for all Synchronous Mode slaves.
- If the Synchronous Data IO Mode is enabled through EEPROM setting (*Synchronous_Data_IO* = '1', *P2_Sync_Activation* = '0'), the **first DEXG call** that is received by a particular slave after the activation of the Data Port (*Data_Exchange_Disable* flag was cleared by a WPAR call) is processed like in regular operation. This is to capture decent input data for the first slave response and to activate the outputs as fast as possible.

The Data I/O operation is repeated together with the I/O cycle of the other *Synchronous Mode* slaves in the network at the common trigger event. By that, the particular slave has fully reached the *Synchronous Mode.*

- If the ***P2_Sync_Activation*** **flag is set to '1'** the Synchronous Data IO Mode can be activated or deactivated during normal operation by sending Write_Parameter calls containing the appropriate value in P2 (see Table 23).

  If the P2 output register changes from '1' to '0' the Synchronous Data IO Mode gets enabled in the first instance. Real synchronous data I/O operation is reached after reception of the next DEXG call addressing the slave and the occurrence of the common trigger event. As in standard operation (Synchronous Data IO Mode is activated by EEPROM setting) the first DEXG still processes a data IO operation immediately. This is to capture decent input data for the slave response and to activate the outputs as fast as possible.

  The Data I/O operation is repeated together with the I/O cycle of the other *Synchronous Mode* slaves in the network at the common trigger event. By that, the particular slave has fully reached the *Synchronous Mode.*

  If the P2 output register changes from '0' to '1' the Synchronous Data IO Mode gets deactivated and disabled immediately. In case a synchronous data I/O event was already scheduled but not yet processed (armed but no fired) before the Synchronous Data I/O Mode became deactivated, the associated data output value gets lost.

  Reactivation of the Synchronous Data I/O Mode occurs in same manner as described above if P2 changes back to '0'.

- To avoid a general suppression of Data I/O in the special case that a slave in *Synchronous Mode* receives **DEXG calls only to its own address** (i.e. employment of a handheld programming device), the *Synchronous Mode* becomes deactivated, once the SAP5 receives three consecutive DEXG calls to its own slave address. The IC resumes to *Synchronous Mode* operation after it observed a DEXG call to a different slave address then its own. The reactivation of the *Synchronous Mode* is handled likewise for the first DEXG call after activation of the Data Port or after activation of the Synchronous Data I/O Mode by P2 changing to '0' (see description above).

If any of the data ports D0..D3 is configured as pure output (named OUT in Table 25 on page **Fehler! Textmarke nicht definiert.**), the SAP5 returns the output data that was received from the master immediately back in its slave response. Since there is no input function available at such port, the return value is independent from a possible *Synchronous Mode* operation.

Running in Synchronous Mode, the SAP5 generates the Data Strobe (DSTBn) signal as well, whereas the timing of input sampling and output buffering exactly corresponds to the regular operation (refer to Figure 7 and Table 21).

4.8.4 Support of 4I/4O Signaling in Extended Address Mode

In Extended Address Mode the information bit I3 of the AS-i master telegram is used to distinguish between A- and B-slaves that operate in parallel at the same AS-i slave address. For more detailed information refer to [1] AS-i Complete Specification.

Besides the benefit of an increased address range, the cycle time per slave is increased in Extended Address Mode from 5 ms to 10 ms and the useable output data is reduced from 4 to 3 bits. Because of the later, Extended Address Mode slaves can usually control a maximum of 3 data outputs only. The input data transmission is not effected since the slave response still carries 4 data information bits in Extended Address Mode.

Additionally, the SAP5 supports applications that require 4 bit wide output data in Extended Address Mode, but can tolerate further increased cycle times (i.e. push buttons and pilot lights). Such applications shall be directly characterized by a new Slave Profile 7.A.x.7 that is to be defined in the AS-i Complete Specification.

If the IC is operated in Extended Address Mode and the *Ext_Addr_4I/4O_Mode* flag is set (='1') in the E²PROM (refer to Table 9) it treats information bit I2 as selector for two 2-bit wide data output banks:

- *Bank_1 = D0/D1*
- *Bank_2 = D2/D3*.

A master shall consecutively transmit data to *Bank_1* and *Bank_2*, toggling the information bit I2 in the respective master calls. However, the SAP5 triggers a data output event (modification of the Data Output Ports and generation of Data Strobe) as follows:

- If the *Parallel_Out_4I/4O* flag is set (='1') in the E²PROM (refer toTable 9) the SAP5 triggers a data output event only if information bit I2 is equal to '0'. By that, new output data is issued at the Data Port synchronously for both banks at the same time.
- If the *Parallel_Out_4I/4O* flag is not set ('0') the SAP5 triggers a data output event at every cycle. However, depending on the information bit I2 only one bank of the Data Port gets refreshed.

Following coding applies:

Table 24: Meaning of master call bits I0 … I3 in *Ext_Addr_4I/4O_Mode*

Master Call Bit	Operation / Meaning			
	Parallel_Out_4I/4O = '0'		*Parallel_Out_4I/4O* = '1'	
	I2 = '0'	I2 = '1'	I2 = '0'	I2 = '1'
I0	D2 = I0	D2 = unchanged	D2 = I0	D2 = unchanged [1]
I1	D3 = I1 D1 = unchanged D0 = unchanged	D3 = unchanged D1 = I1 D0 = I0	D3 = I1 D1 = *DO1_tmp* [2] D0 = *DO0_tmp* [2]	D3 = unchanged [1] D1 = unchanged [1] D0 = unchanged [1] *DO1_tmp* = I1 *DO0_tmp* = I0
I2	I2: /Sel-bit for transmission to *Bank_1* (D0/D1) / *Bank_2* (D2/D3)			
I3	I3: /Sel-bit for A-Slave/B-Slave addressing			

NOTES:

[1] If I2 = '1' then I0/I1 are directed to temporary data output registers *DO0_tmp*/*DO1_tmp*

[2] If I2 = '0' then I0/I1 are directed to the data output registers D2/D3 and *DO0_tmp*/*DO1_tmp* are directed to the data output registers D0/D1

In order to ensure that both *Bank_1* and *Bank_2* data are refreshed continuously, the SAP5 supervises the alternation of the I2 Sel-bit by use of the 4I/4O Watchdog. The 4I/4O Watchdog gets activated as soon as

- The Communication Watchdog is activated (refer to Table 33).
- The IC is operated in Extended Address Mode and the *Ext_Addr_4I/4O_Mode* flag is set (='1') in the E²PROM.
- Slave address is unequal to zero (0).
- No E²PROM write access is active.
- The slave is activated, i.e. the *Data_Exchange_Disable* flag is cleared.

If there is no alternation of the I2 bit for more than 327ms (+16ms) ms after the activation of the slave the 4I/4O Watchdog takes the following actions:

- It generates Data and Parameter Strobe signals at the DSTBn an PSTBn pins with timing according to Figure 6 and Figure 7.
- After DSTBn an PSTBn strobe generation finished, the 4I/4O Watchdog invokes an unconditioned IC Reset. It sets the *Data_Exchange_Disable* flag and - afterwards - starts the IC initialization procedure, switching all Data and Parameter Outputs inactive.

Input data is captured and returned to the master at every cycle, independent of the value of information bit I2

4.8.5 Special function of DSTBn

Beside its standard output function the Data Strobe Pin serves as external reset input for all operational modes of the IC. Pulling the DSTBn pin LOW for more than a minimum reset time generates an unconditioned reset of the IC, which is immediately followed by an initialization of the state machine (E²PROM read out).

Further information on the IC reset behavior, especially in regard to the signal timing, can be found at chapter 4.13 IC Reset.

4.9 Data and Parameter Port Configuration

Data and Parameter ports are configured by programming the *IO_Code* in the E²PROM. Moreover, the configuration also depends on the *Safety_Mode_Enable* settings.

NOTE: Below Table 25 refers to slaves **not** running in Safety Mode (refer to chapter 4.18)

The following configurations are possible:

- **OUT**: output only, data are valid up to the next DSTBn/PSTBn strobe pulse
- **IN**: input only, open drain output is fixed at high-impedance state
- **I/O**: bi-directional port with timing according to Figure 6 and Figure 7
- **INOUT**: In case *IO_Code* = 7 Parameter ports are configured inputs after *WPAR* master calls and outputs after *DEXG* master calls, respectively.
- **PASSIV**: no input function and open drain output is fixed at high-impedance state

If one of the data ports D0…D3 is configured as OUT, the SAP5 slave answer to a *DEXG* master request contains the respective information bit I0...I3 received from the master. However, parameter ports P0...P3 are always operated bi-directional, including a read-back of the actual port level as described in chapter 4.8 on page 28.

Table 25: Data and Parameter Port Configuration for Non-Safety-Mode Operation

IO_Code	D0	D1	D2	D3 [1]	P0	P1	P2	P3 [1]
0	IN	IN	IN	IN	OUT	OUT	OUT	OUT
1	IN	IN	IN	OUT	OUT	OUT	OUT	OUT
2	IN	IN	IN	I/O	OUT	OUT	OUT	OUT
3	IN	IN	OUT	OUT	OUT	OUT	OUT	OUT
4	IN	IN	I/O	I/O	OUT	OUT	OUT	OUT
5	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT
6	IN	I/O	I/O	I/O	OUT	OUT	OUT	OUT
7 [2]	OUT	OUT	OUT	OUT	INOUT	INOUT	INOUT	INOUT
8	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
9	OUT	OUT	OUT	IN	OUT	OUT	OUT	OUT
A	OUT	OUT	OUT	I/O	OUT	OUT	OUT	OUT
B	OUT	OUT	IN	IN	OUT	OUT	OUT	OUT
C	OUT	OUT	I/O	I/O	OUT	OUT	OUT	OUT
D	OUT	IN	IN	IN	OUT	OUT	OUT	OUT
E	OUT	I/O	I/O	I/O	OUT	OUT	OUT	OUT
F [3]	PASSIV	PASSIV	PASSIV	PASSIV	OUT	OUT	OUT	OUT

[1] Slaves running in *Extended_Address_Mode* (*ID_Code* = 0xA) will output the respective select bit (I3) at the P3 pin and at the D3 pin in case it is configured as OUT or I/O.

[2] The special case *IO_Code* = 0x7 causes the Parameter Ports acting as Data Inputs after *DEXG* master calls. Thus a bi-directional data exchange with separate data inputs and outputs is possible. Parameter Ports are always outputs after *WPAR* master calls.

NOTE: *IO_Code* = 0x7 is not allowed for the SAP5 16 Pin version.

[3] There is no data exchange possible in case *IO_Code* = 0xF, i.e. Data Outputs are always at high impedance state, no slave answer is generated for received *DEXG* master calls.

Table 26: Data and Parameter Port Configuration in Safety Mode

Package Version	IO_Code	D0	D1	D2	D3	P0	P1	P2	P3 [1]
16 Pin	0…6, 8…F	F-D0* IN	D0* OUT	F-D2* IN	D2* OUT	don't care	don't care	don't care	don't care
16 Pin	7 [1]	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care
20 Pin	0…6, 8…F	F-D0* IN	D0* OUT	F-D2* IN	D2* OUT	P0 OUT	P1 OUT	P2 OUT	P3 OUT
20 Pin	7 [2]	D0 OUT	D1 OUT	D2 OUT	D3 OUT	F-D0* IN P0 OUT	D0* OUT P1 OUT	F-D2* IN P2 OUT	D2* OUT P3 OUT

[1] *IO_Code* = 0x7 is not allowed for the SAP5 16 Pin version.

[2] Parameter Ports are parameter outputs during *WPAR* master calls and after *DEXG* master calls. They are in high impedance state after *WPAR* master calls and act as input when a *DEXG* master calls is performed.

4.10 Fault Indication Input PFAULT

The fault indication input PFAULT is provided for sensing a periphery fault-messaging signal. It contains a high voltage high impedance input stage that sets the status bit S1 of the AS-i Slave to '1' if it detects a LOW level at the PFAULT pin. DC properties of the pin are specified at Table 16.

Signal transitions at the PFAULT pin become visible in S1 with a slight delay, because a clock synchronizing circuit is located in between.

4.11 LED outputs

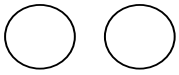
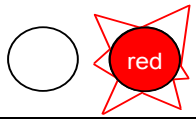
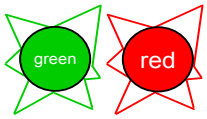
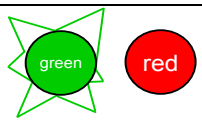
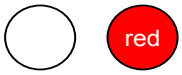
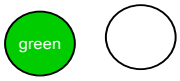
4.11.1 Slave Mode

The SAP5 provides two LED pins for enhanced status indication. LED1 and LED2 both comprise NMOS open drain output drivers. In addition, LED2 contains a high voltage high impedance input stage for purposes of the IC production test.

In order to comply with the signaling schemes defined in the AS-i Complete Specification a **red LED** shall be connected to **LED2** and a **green LED** shall be connected to **LED1.**

Following status indication is supported

Table 27: LED status indication

Priority / Status	LED1 / LED 2	Note
1. Power Off		No power supply available
2. External Reset		DSTRBn driven LOW for more than 90ms.
3. Periphery Fault	 alternating	Periphery Fault signal generated at PFAULT input.
4. No data exchange (Address = 0)		Slave is waiting for address assignment. Data Port communication is not possible.
5. No data exchange		The IC was reset by the Communication Watchdog or by RES or BR01 master calls, thus the *Data_Exchange_Disable* flag is still set, prohibiting Data Port communication. IC is waiting for a *Write_Parameter* request. [1]
6. Normal operation		Data communication is established

[1] This status is not signaled if the Communication Watchdog is not activated (refer to chapter 4.17 Communication Monitor/Watchdog).

The flashing frequency of any flashing status indication is **2 … 3 Hz**.

In case of the simultaneous occurrence of several states the status with the highest priority is signaled.

4.11.2 Master/Repeater Mode

In Master/Repeater Mode LED1 provides the Manchester-II-coded, re-synchronized equivalent of the telegram signal received at the AS-i input channel.

Every received AS-i telegram is checked for consistency with the protocol specifications and timing jitters become removed as long as they stay within the specified limits. In case a telegram error is detected, the output becomes inactive for a certain time periode, see chapter 4.19.3.

LED2 is always logic HIGH (high impedance) in Master/Repeater. In such applications, the green LED shall be connected to Pin UOUT or different supply levels.

4.12 Oscillator Pins OSC1, OSC2

Table 28: Oscillator pin parameters

Symbol	Parameter	Min	Max	Unit	Note
V_{OSC_IN}	Input voltage range	-0.3	V_{U5R}	V	
C_{OSC}	External parasitic capacitor at oscillator pins OSC1, OSC2	0	8	pF	
$C_{CRYSTAL}$	Crystal load capacitance	0	12	pF	
V_{IL}	Input "low" voltage	0	1.5	V	[1]
V_{IH}	Input "high" voltage	3.5	V_{U5R}	V	[1]

[1] for external clock applied to OSC1

The oscillator supports direct connection of 5.33 MHz or 16.000 MHz crystals with a dedicated load capacity of 12pF and parasitic pin capacities of up to 8pF. The IC automatically detects the oscillation frequency of the connected crystal and controls the internal clock generator circuit accordingly.

The oscillator unit also contains a clock watch dog circuit that can generate an unconditioned IC reset if there was no clock oscillation for more than about 20µs. This is to prevent the IC from unpredicted behavior if no clock signal is available anymore.

4.13 IC Reset

Any IC reset turns the Data Output and Parameter Output Registers to 0xF and forces the corresponding output drivers to high impedance state. Except at Power On Reset, Data Strobe and Parameter Strobe signals are simultaneously generated to visualize possibly changed output data to external circuitry.

The *Data_Exchange_Disable* flag becomes set during IC reset, prohibiting any data port activity right after IC initialization and as long as the external circuitry was not pre-conditioned by decent parameter output data. Consequently the AS-i master has to send a *Write_Parameter* call in advance of the first *Data_Exchange* request to an initialized slave. Following IC initialization times apply:

Table 29: IC Initialization times

Symbol	Parameter	Min	Max	Unit	Note
t_{INIT}	Initialization time after Software Reset (generated by master calls *Reset_Slave* or *Broadcast_Reset*) or external reset via DSTBn		2	ms	[1]
t_{INIT2}	Initialization time after power on		30	ms	[2]
t_{INIT3}	Initialization time after power on with high capacitive load		1000	ms	[3]

[1] guaranteed by design

[2] 'power on' starts latest at V_{UIN} = 18V, external capacitor at pin UOUT less than or equal 10µF

[3] C_{UOUT} = 470µF, t_{INIT3} is guaranteed by design only

4.13.1 Power On Reset

In order to force the IC into a defined state after power up and to avoid uncontrolled switching of the digital logic if the 5V supply (U5R) breaks down below a certain minimum level, a Power On Reset is executed under the following conditions:

Table 30: Power On Reset Threshold Voltages

Symbol	Parameter	Min	Max	Unit	Note
V_{POR1F}	V_{U5R} voltage to trigger internal reset procedure, falling voltage	1.2	1.7	V	[1]
V_{POR1R}	V_{U5R} voltage to trigger INIT procedure, rising voltage	3.5	4.3	V	[1]
t_{Low}	Power-on reset pulse width	4	6	µs	

[1] guaranteed by design

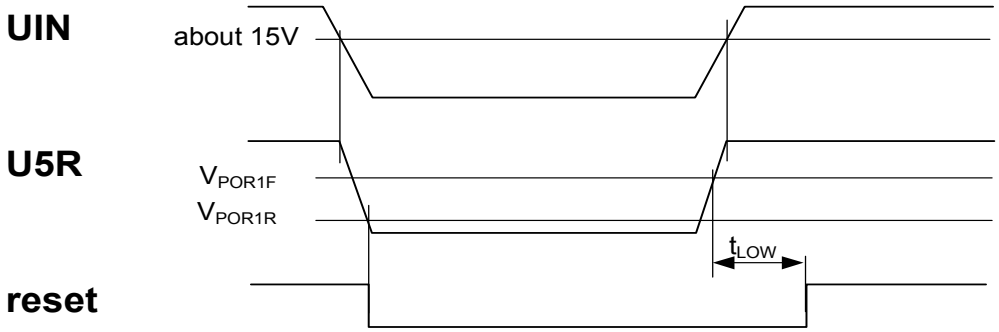


Figure 9: Power-On Behavior (all modes)

Note: The power-on reset circuit has a threshold voltage reference. This reference matches the process tolerance of the logic levels and must not be very accurate. All values depend slightly on the raise and fall time of the supply voltage.

4.13.2 Logic controlled Reset

The IC also becomes reset after reception of *Reset_Slave* or *Broadcast_Reset* commands, expiration of the (enabled) Communication Watchdog or entering of a forbidden state machine state (i.e. due to heavy EMI).

4.13.3 External Reset

The IC can be reset externally by pulling the DSTBn pin LOW for more than a minimum reset time. The external reset input function is provided in every operational mode of the IC – Slave Mode and Master/Repeater Mode. The following signal timings apply:

Table 31: Timing of external reset

Symbol	Parameter	Min	Max	Unit	Note
$t_{noRESET}$	DSTBn LOW time for no reset initiation		90	ms	
t_{RESET}	Reset execution time, DSTBn H/L transition to Hi-Z output drives at DO0...DO3, P0…P3		99	ms	
t_{INIT}	State Machine initialization time after reset (E²PROM read out)		2	ms	

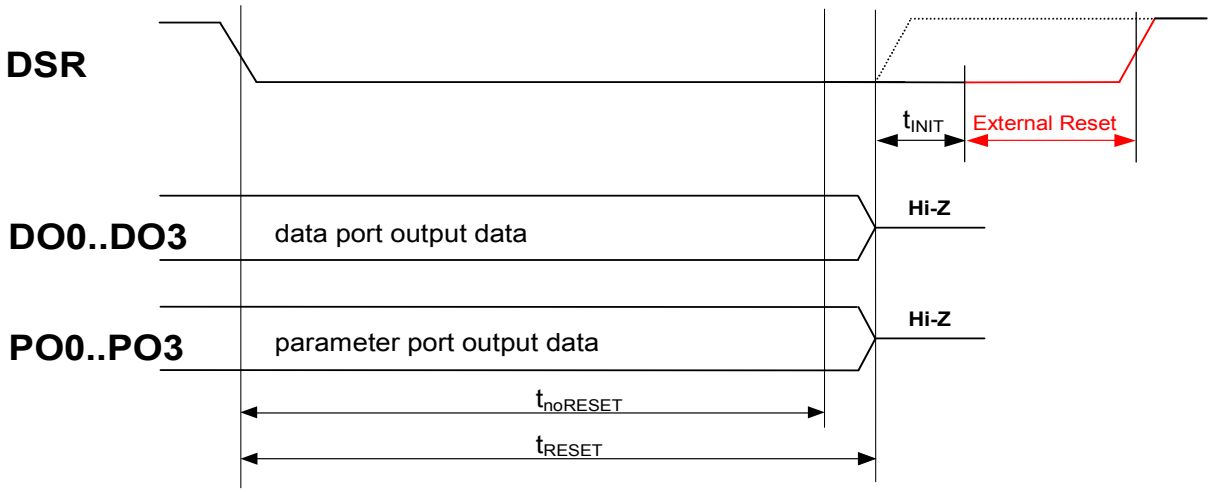


Figure 10: **Timing diagram external Reset via DSTBn**

The external reset is generated “edge sensitive” to the expiration of the t_{RESET} timer. The initialization procedure is starting immediately after the event, independent of the state of DSTBn. The external reset state lasts if DSTBn still remains LOW after $t_{RESET} + t_{INIT}$. The corresponding error state display is described in chapter 4.11.

4.14 UART

The UART performs a syntactical and timing wise analysis of the received telegrams at the AS-i input channel. It converts the pulse coded AS-i input signal into a Manchester-II-coded bit stream and provides the receive register with decoded telegram bits. The UART also realizes the Manchester-II-coding of a slave answer.

In Master/Repeater Mode the output signal of the Manchester coder (AS-i pulse to MAN signal conversion) is resynchronized and forwarded to pin LED1. Any pulse timing jitters of the received AS-i signal become removed, as long as they stay within the specified maximum limits. If the received AS-i telegram does not pass one of the different error checks (see detailed description below), the LED1 output the output becomes inactive for a certain time periode, see chapter 4.19.3.

The comparator stages at the AS-i-line receiver generate two pulse-coded output signals (*p_pulse*, *n_pulse*) disjoining the positive and negative telegram pulses for further processing. To reduce UART sensitivity on erroneous spike pulses, pulse filters suppress any *p_pulse*, *n_pulse* activity of less than 750 ns width.

After filtering, the *p_pulse* and *n_pulse* signals are checked in accordance with the AS-i Complete Specification for following telegram transmission errors:

Start_bit_error — The initial pulse following a pause must have negative polarity. Violation of this rule is detected as *Start_bit_error*. The first pulse is the reference for bit decoding. The first bit detected shall be of the value 0.

Alternating_error — Two consecutive pulses must have different polarity. Violation of this rule is detected as *Alternating_error*.

Note: A negative pulse shall be followed by a positive pulse and vice versa.

Timing_error — Within any master request or slave response, the digital pulses that are generated by the receiver are checked to start in periods of $(n * 3\mu s)^{+1.500\mu s}_{-0.875\mu s}$ after the start of the initial negative pulse, where n = 1 ... 26 for a master request and n = 1 ... 12 for a slave response. Violation of this rule is detected as *Timing_error*.

Note: There is a certain pulse timing jitter associated with the receiver output signals (compared to the analog signal waveform) due to sampling and offset effects at the comparator stages. In order to take the jitter effects into account, the timing tolerance specifications differ slightly from the definitions of the AS-i Complete Specification.

No_information_error — Derived from the Manchester-II-Coding rule, either a positive or negative pulse shall be detected in periods of $(n * 6\mu s)^{+1.500\mu s}_{-0.875\mu s}$ after the start of the initial negative pulse, where n = 1 ... 13 for a master request and n = 1 ... 6 for a slave response. Violation of this rule is detected as *No_information_error*.

Note: The timing specification relates to the receiver comparator output signals. There is a certain pulse timing jitter in the digital output signals (compared to the analog signal waveform) due to sampling and offset effects at the comparator stages. In order to take the jitter effects into account, the timing tolerance specifications differ slightly from the definitions of the AS-i Complete Specification.

Parity_error — The sum of all information bits in master requests or slave responses (excluding start and end bits, including parity bit) must be even. Violation of this rule is detected as *Parity_error.*

End_bit_error — The pulse to be detected $(n * 6\mu s)^{+1.500\mu s}_{-0.875\mu s}$ after the start pulse shall be of positive polarity, where n = 13 (78 µs) for a master request and n = 6 (36 µs) for a slave response. Violation of this rule shall be detected as an *End_bit_error.*

Note: This stop pulse shall finish a master request or slave response.

Length_error — Telegram length supervision is processed as follows. If during the first bit time after the end pulse of a master request (equivalent to the 15th Bit time) for synchronized slaves (during the first three bit times for not synchronized slaves, equivalent to the Bit times 15 to 17) or during the first bit time after the end pulse of a slave response (equivalent to the 8th Bit time) a signal different from a pause is detected, a *Length_error* is detected.

If at least one of these errors occurs, the received telegram is treated invalid. In this case, the UART will not generate a Receive Strobe signal. It moves to asynchronous state and wait for a pause at the AS-i line input. After a pause was detected, the UART is ready to receive the next telegram.

Receive Strobe signals are generally used to validate the correctness of the received data. Receive Strobe starts the internal processing of a master request. If the UART was in asynchronous state before the signal was generated, it transforms to synchronous state thereafter. In case the received slave address matches the stored address of the IC, the transmitter is turned on by the Receive Strobe pulse, letting the output driver settle smoothly at the operation point (avoiding false pulses at the AS-i line).

4.15 Main State Machine

The Main State Machine controls the overall behavior of the IC. Depending on the configuration data stored in the E²PROM, the State Machine activates one of the different IC operational modes and controls the digital I/O ports accordingly. In Slave Mode it processes the received master telegrams and computes the contents of the slave answer, if required. Table 6 on page 15 lists all master calls that are decoded by the SAP5 in Slave Mode.

To prevent the critical situation in which the IC gets locked in a not allowed state (i.e. by imission of strong electromagnetic radiation) and thereby could jeopardize the entire system, all prohibited states of the state machine will lead to an unconditioned logic reset which is comparable to the AS-i call ”Reset Slave (RES)”.

4.16 Status Registers

Table 32 shows the SAP5 status register content. The use of status bits S0, S1 and S3 is compliant to the AS-Interface Complete Specification. Status bit S2 is not used. The status register content can be determined by use of a *Read_Status* (*RDST*) master request (refer to Table 6).

Table 32: Status Register Content

Status Register Bit	Sx = 0	Sx = 1
S0	E^2PROM write accessible	Slave Address stored volatile and/or E^2PROM access blocked (write in progress) [1]
S1	no periphery fault detected, (input PFAULT = ‘1’), E^2PROM Firmware Area and Safety Area content consistent	periphery fault detected, (input PFAULT = ‘0’), parity bit error in E^2PROM Firmware Area or Safety Area
S2	Static zero	N/A
S3	E^2PROM content consistent	E^2PROM contains corrupted data

[1] Status Bit S0 is set to ‘1’ as soon as a *DELA* master request was received and the slave address was unequal to “0” before. Additionally, it is set for the entire duration of each E^2PROM write access.

4.17 Communication Monitor/Watchdog

The IC contains an independent Communication Monitor that observes the processing of *Data_Exchange* (*DEXG*) and *Write_Parameter* (*WPAR*) requests. If no such requests have been processed for more than 94.2ms (+4ms) the Communication Monitor recognizes a No Data/Parameter Exchange status and turns the red status LED (LED2) on. Any following *Data_Exchange* or *Write_Parameter* request will let the Communication Monitor start over and turn the red status LED off.

The Communication Monitor is only activated at slave addresses unequal to zero (0) and while the IC is processing the first *Write_Parameter* request after initialization. It becomes deactivated at any IC Reset or after the reception of a *Delete_Address* Request.

Activation of the Communication Watchdog depends on several E²PROM flags and the Parameter Port P0 Output Register

Note: The value of the Parameter Port P0 Input does not influence the watchdog activation at all. Only the master can change the activation status by sending a corresponding **Write_Parameter** (WPAR) request. This allows to use the feature even if IO-Code 7 is selected. In this case, the parameter port pins are mapped into Data

Input pins. But since the activation of the Communication Watchdog only depends on the value of the parameter output register, the watchdog functionality still remains controlled by the master.

Watchdog activation through the value of Parameter Port P0 is not available in Safety Mode.

Table 33: Activation of the SAP5 *Communication Watchdog*

Lock_EE_PRG E²PROM flag	*Inhibit_Watchdog* E²PROM flag	*P0_Watchdog_Activation* E²PROM flag	*Safety_Mode _Enable*	Parameter Port P0 output reg	*Watchdog Activation*
0	X	X	X	X	**OFF**
1	1	X	X	X	**OFF**
1	0	0	X	X	**ON**
1	0	1	1	X	**ON**
1	0	1	0	0	**OFF**
1	0	1	0	1	**ON**

The Communication Watchdog recognizes a No Data Exchange status as soon as the following conditions come true together:

- The Communication Watchdog is activated.
- No DEXG or WPAR request was processed for more than 94.2ms (+4ms).
- Slave address is unequal to zero (0).
- No E²PROM write access is active.

If the Communication Watchdog detects a No Data Exchange status, it takes the following actions:

- It concurrently generates Data and Parameter Strobe signals at the DSTBn an PSTBn pins with timing according to Figure 6 and Figure 7. NOTE: At this time, the data and parameter output values still comply with the values received with the last *DEXG* and *WPAR* master call, respectively.
- After DSTBn an PSTBn strobe generation finished, the Communication Watchdog invokes an unconditioned IC Reset. It sets the *Data_Exchange_Disable* flag and - afterwards - starts the IC initialization procedure, switching all Data and Parameter Outputs inactive.

In order to resume to normal Data Port communication after a Watchdog IC Reset, the *Data_Exchange_Disable* flag must be cleared again. Therefore, the master has to send a *WPAR* request again before Data Port communication can be reestablished. This ensures new parameter setup of possibly connected external circuitry.

The state until the *Data_Exchange_Disable* flag returns to '0' is signaled by a certain LED1 and LED2 status indication (refer to 4.11).

4.18 Safety Mode

Using the SAP5 Safety Mode makes it easy to implement a safety-related AS-i slave according to the AS-i Safety at Work concept. Slaves complying with the control category 4 according to EN 954 –1 can be implemented even with a minimum of external circuitry.

The Safety Mode is active as soon as the E²PROM flag *Safety_Mode_Enable* is set to '1' (logic HIGH). Thus, it is basically independent on the slave profile, whereas the assignment of the 3-level-input pins mentioned below to either the Data- or the Parameter port depends on the *IO_Code* as described in Table 26 on page 34.

Furthermore, in order to fulfill certain security requirements, the Safety Mode is not combinable with one or more of the following SAP5 features:

- Delay Mode (chapter 4.8.2)
- Synchronous Mode (chapter 4.8.3)
- Ext_Addr_4I/4O_Mode (chapter 4.8.4)
- P0 Watchdog Activation (chapter 4.17)

The Safety Mode of the SAP5 IC is of relevance to the actions following an *DEXG* master request. Instead of the regular input data provided at the data ports, a 4-bit data word from a specific 8 * 4 bit code table as described in [2] is transmitted to the master. Cycling the code table is used to transmit another data word with each *DEXG* master call.

In order to meet certain safety requirements the data words transmitted to the master pass through a special pre-processing. Therefore, the code table stored within the Safety Area of the E²PROM (refer to Table 11 on page 21) does not match the reference code table as specified in [2] but is derived from a special coding scheme as described below.

Table 34: Example for Cryptographic Code Table

Reference Code Table				Step 1 cycle D0/D2 by one cycle				Step 2 invert D0/D2				Step 3 : swap D1 – D3 Code Table written to the E²PROM				
D3	D2	D1	D0	D3	D2	D1	D0	D3	D2*	D1	D0*	D3*	D2*	D1*	D0*	*swap_flag*
0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1
0	1	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0
0	1	1	0	0	0	1	1	0	1	1	0	1	1	0	0	1
1	0	0	1	1	1	0	0	1	0	0	1	1	0	0	1	0
1	1	1	0	1	0	1	1	1	1	1	0	1	1	1	0	0
1	0	1	1	1	1	1	0	1	0	1	1	1	0	1	1	1
1	1	0	0	1	1	0	1	1	0	0	0	0	0	1	0	1
0	1	1	1	0	0	1	1	0	1	1	0	0	1	1	0	0

The E²PROM code table has to be derived from a Reference Code Table which meets the requirements of [2] as follows:

1. Looking up to the Reference Code Table, the data bit vectors D0 and D2 are scrolled forward by one cycle. Refer to Table 34 for an example.
2. Data bit vectors D0 and D2 are inverted and stored as D0* and D2* in the E²PROM.
3. Four out of eight data bits from the vector D1 are interchanged with the respective data bits from vector D3. The respective bits are marked with *swap_flag* = '1'. Unchanged data bit pairs are marked with *swap_flag* = '0'. Coded in such a way, the vectors are stored as D1* and D3* in the E²PROM .
4. The additional *swap_flag* attached to each data word is stored in the E²PROM as well.

Running in Safety Mode, the E²PROM data bits D0* and D2* are put out at the port D1/D3 or P1/P3, respectively (for port configuration refer to Table 26 on page 34). An external circuit has to invert these signals, it adds a voltage offset (refer to Figure 12) and delays it for about 20µs. Thus the data actually will be transmitted with the following AS-i cycle. Furthermore, the safety-related switches are connected between the external circuitry and the SAP5 safety inputs F-D0* and F-D2* (refer to Figure 11).

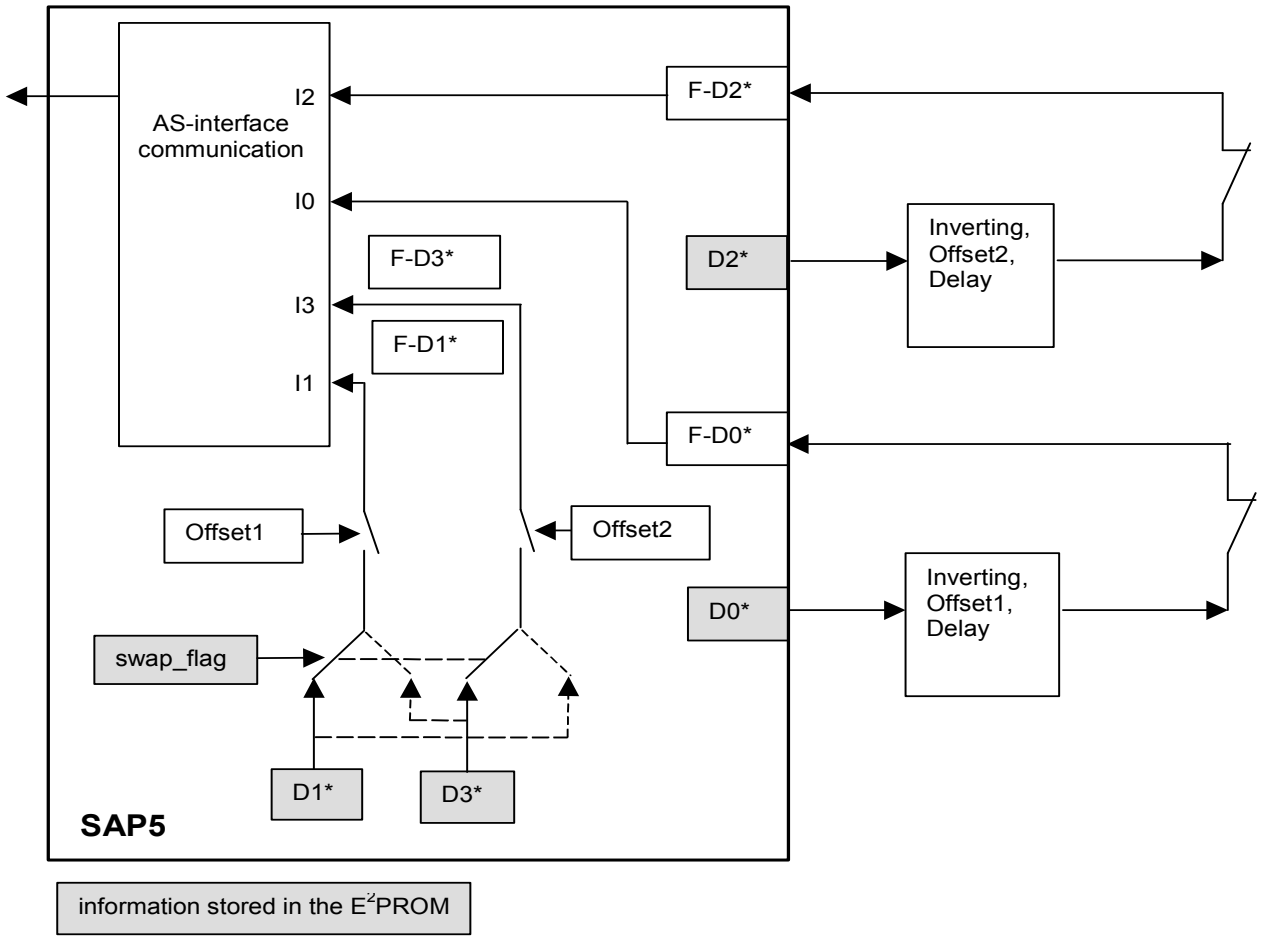


Figure 11: Safety Mode Data Processing

The special input ports F-D0* and F-D2* act as 3-level-input pins in Safety Mode. In order to ensure proper decoding of input data, the voltages must satisfy requirements as specified in below Figure 12 and Table 16 on page 25, respectively.

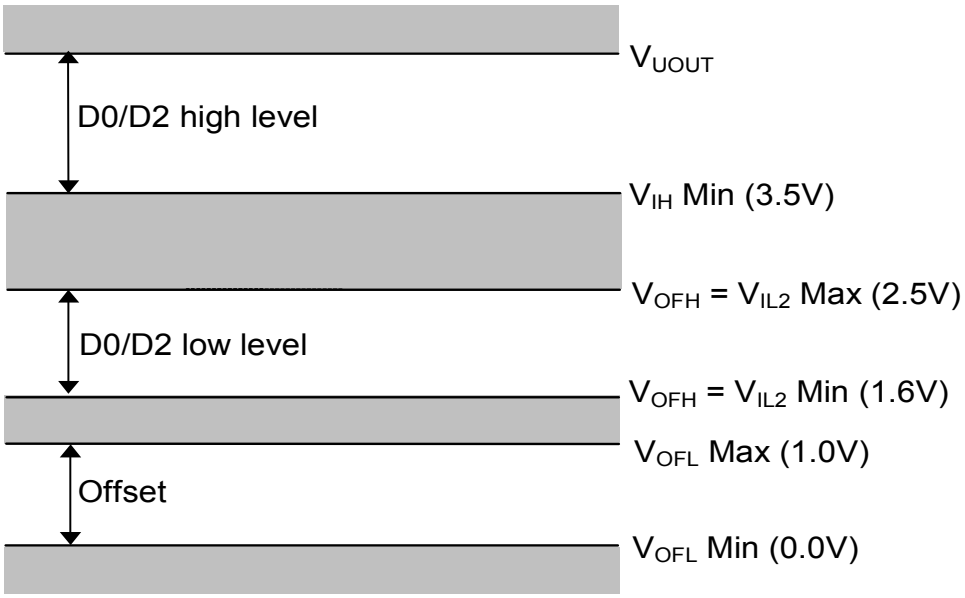


Figure 12: Data Input Voltage Constraints in *Safety Mode*

As soon as the F-D0* input pad detects an offset level less than V_{OFL}(Max) the SAP5 resets the data input for D1 (F-D1*), signalling an OPEN state at the safety switch connected to D0*. The input data for D3 (F-D3*) will be reset if the F-D2* detects an offset level less than V_{OFL}(Max), respectively.

Provided that the offset levels are not missing, the E^2PROM bits D1* and D3* are transmitted as data bits D1 and D3 if *swap_flag* = '0', otherwise they are swapped.

In order to avoid desynchronization with the safety monitor in case the AS-i master repeats a *DEXG* call, the SAP5 will not update the data code word for 224µs (+16µs) after a *DEXG* call had been processed.

4.19 Master- and Repeater Mode

4.19.1 Master/ Repeater Mode Activation

The SAP5 Master/ Repeater Mode functionality gets enabled by use of the E²PROM flag *Master_Mode* (refer to Table 9). In order to activate the *Master_Mode*, an IC Reset (refer to chapter 4.13 on page 36) has to be performed after programming of the E²PROM *Master_Mode* flag.

For distinction between Master- and Repeater Mode the *ID_Code* may be set to a certain value as described in Table 35.

NOTE: The *ID_Code* has to be programmed **before** activation of the *Master_Mode* flag. Once the *Master_Mode* flag is set to logic HIGH, the slave functionality of the SAP5 is no longer available, preventing any write access to the E²PROM by use of AS-i master requests as described on page 20.

Moreover, the Master- and Repeater Mode functionality may be disabled generally by use of a hidden E²PROM flag. This flag is inaccessible by the user, but may be set during the ZMD production test.

Table 35: Activation of the SAP5 *Master/Repeater Mode*

Master_Mode E²PROM flag	*ID_Code*	Master Mode 1	Master Mode 2	Repeater Mode
0	X	**OFF**	**OFF**	**OFF**
1	0…4	**ON**	**OFF**	**OFF**
1	6…0xF	**OFF**	**ON**	**OFF**
1	5	**OFF**	**OFF**	**ON**

4.19.2 Pin Assignment

In Master- and Repeater Mode the SAP5 pins are configured as follows. Pins which are not used are kept at logic HIGH (high impedance) state in order to reduce internal power dissipation of the IC.

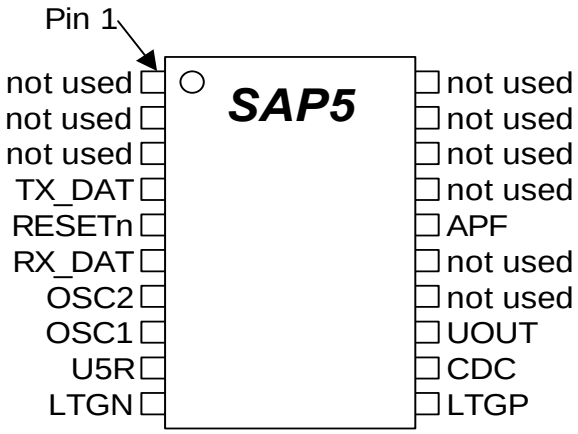


Figure 13: SAP Package Pin Assignment in Master/Repeater Mode

Table 36: SAP5 Pin Assignment in Master- and Repeater Mode

SOIC 20 Pin #	SOIC 16 pin #	Name	Signal Name	Pin configuration	Description
			in Master/Repeater Mode		
1	-	P1	none	I/O	not used
2	-	P0	none	I/O	not used
3	1	D1	none	I/O	not used
4	2	D0	TX_DAT	IN	transmit signal (Manchester II signal)
5	3	DSTBn	RESETn	IN	external reset input (active LOW)
6	4	LED1	RX_DAT	OUT	receive signal (Manchester II signal)
7	5	OSC2	OSC2	OUT	Crystal oscillator
8	6	OSC1	OSC1	IN	Crystal oscillator / External clock input
9	7	U5R	U5R	OUT	Regulated 5V power supply
10	8	LTGN	LTGN	IN	AS-i Transmitter/Receiver output, to be connected to AS-i-
11	9	LTGP	LTGP	IN	AS-i Transmitter/Receiver input, to be connected to AS-i+ via reverse polarity protection diode, input for the power fail comparator
12	10	CDC	CDC	OUT	external buffer capacitor
13	11	UOUT	UOUT	OUT	decoupled actuator/sensor power supply
14	12	PFAULT	none	IN	not used
15	13	LED2	none	OUT	not used
16	14	PSTBn	APF	OUT	AS-I power fail signal
17	15	D3	none	I/O	not used
18	16	D2	none	I/O	not used
19	-	P3	none	I/O	not used
20	-	P2	none	I/O	not used

4.19.3 Functional Description

In Master/Repeater Mode the SAP5 provides a simple physical-layer interface function between the AS-I line and an external binary channel.

The signal RX_DAT represents the Manchester-II-coded, re-synchronized equivalent of the telegram signal received at the AS-i input channel. Polarity of that bitstream depends on the programmed operation mode according to Table 37.

Table 37: Functional Distinctions of SAP5 *Master- and Repeater Mode*

	Modulation of signal RX_DAT in case of ASI Power Fail	Loopback Mode	Polarity of signal RX_DAT
Master Mode 1	**ON**	**ON**	**active HIGH**
Master Mode 2	**OFF**	**ON**	**active HIGH**
Repeater Mode	**OFF**	**OFF**	**active LOW**

Every received AS-i telegram is checked for consistency with the protocol specifications and timing jitters become removed as long as they stay within the specified limits. In case a telegram error is detected, the output signal becomes inactive for a time period defined by t_{BREAK} (refer to Table 39).

The signal TX_DAT is directly forwarded to the AS-i line transmitter avoiding any additional logic delays.

In case the Loopback Mode is not active, the AS-i receiver gets disabled as long as the SAP5 is transmitting an AS-i signal. Otherwise, the transmitted signal is read back in parallel and provided at the RX_DAT output for checkup purposes.

The Loopback time $t_{LOOPBACK}$ is mainly defined by the analog signal processing within the Receiver and the Transmitter. However, an additional delay of up to 1875ns may be inserted if necessary. Therefore, the ID*_Code_Extension_2* EEPROM register has to be programmed as described below.

NOTE: The *ID_Code_Extension_2* has to be programmed **before** programming of the *Master_Mode* flag. Once the *Master_Mode* flag is set to logic HIGH, the slave functionality of the SAP5 is no longer available, preventing any write access to the E²PROM by use of AS-i master requests as described on page 20.

Table 38: Programmable Variation of the Loopback time

ID_Code_Extension_2 (ID2_Bit3 … ID2_Bit0)	$\Delta t_{loopback}$	Unit
0000	0	ns
0001	+125	
0010	+250	
0011	+375	
0100	+500	
0101	+625	
0110	+750	
0111	+875	
1000	+1000	
1001	+1125	
1010	+1250	
1011	+1375	
1100	+1500	
1101	+1625	
1110	+1750	
1111	+1875	

In Master/Repeater Mode the SAP5 provides an AS-i power-fail detector. It consists of a comparator directly connected to the LTGP pin which generates a logic signal in case the voltage at the LTGP pin drops below V_{APF} (refer to Table 39). A subsequent digital signal processing of the comparator output signal is performed as follows:

- An anti-bouncing filter removes each signal states shorter than 6µs. This is to eliminate the influence of AS-i telegrams which are added onto the AS-i DC voltage.
- An additional anti-bouncing filter with different filter times for activation and deactivation of the power-fail signal removes short power-fail pulses.
- The AS-i power-fail signal is provided directly active HIGH as signal APF.
- Additionally, in Master Mode, the AS-i power-fail signal modulates the RX_DAT signal, whereas the active state is signaled by logic HIGH level.

Table 39: Master/Repeater Mode Parameter

Symbol	Parameter	Min	Max	Unit	Note
$t_{loopback}$	Loopback time in *Master Mode*	4.9	6.5	µs	[1]
V_{APF}	AS-i Power Fail voltage threshold	21.5	23.5	V	
$t_{APF\_RX\_DAT}$	minimum activation time for signaling of AS-i Power Fail by use of the RX_DAT signal	640	704	µs	[2]
$t_{APF\_ON\_RX\_DAT}$	release time of the AS-i Power Fail state within the RX_DAT signal	64		µs	[2]
t_{APF_APF}	minimum activation time for signaling of AS-i Power Fail by use of the APF signal	704	768	µs	[2]
t_{HOLD_APF}	AS-i Power Fail hold time	64		µs	
t_{APF_OFF}	delay time after return of the AS-i Power	64	128	µs	
t_{BREAK}	break time in case of an erroneous AS-i signal	9	15	µs	

[1] Loopback time is the time difference between an edge in the MAN code of signal TX_DAT and the corresponding edge in the Manchester-code of the signal RX_DAT. The voltage trigger level for measurement of the edge time is defined by $V_{U5R}/2$. The actual loopback time may be adjusted by programming the *ID_Code_Extension_2* EEPROM register as described in Table 38.

[2] In Master Mode, the AS-i Power Fail state is already signaled by the RX_DAT signal as soon as the power fail condition is true for a time more than $t_{APF\_RX\_DAT}$. However, in order to start the APF minimum hold state (t_{HOLD_APF}), the power fail condition must remain true for another time period defined by $t_{APF\_ON\_RX\_DAT}$. Otherwise, the RX_DAT signal returns to its idle state (logic LOW) immediately.

4.20 Write Protection of ID_Code_Extension_1

The *ID_Code_Extension_1* register of the SAP5 can either be manufacturer configurable or user configurable. As soon as the *Lock_EE_PRG* flag is set, access to the *ID_Code_Extension_1* is handled as follows:

- If the flag *Inhibit_Write_ID1* is set ('1') in the firmware area of the E²PROM, *ID_Code_Extension_1* is manufacturer configurable (refer to Table 9).

  In this case the slave response to a *Read_ID_Code_1* (*RID1*) request is constructed out of the data stored on the internal E²PROM address 2 in User Area of the E²PROM.

  It doesn't matter which data is stored in the *ID_Code_Extension_1* register in E²PROM address 1 in the User Area. The IC will always respond with the protected manufacturer programmed value.

  There is one exception to this principle. If the IC is operated in Extended Address Mode, Bit3 of the returned slave response is taken from the E²PROM address 1 register in the User Area. This is because Bit 3 functions as A/B Slave selector bit in this case and must remain user configurable.

  To ensure consistency of *ID_Code_Extension_1* stored in the data image of Master as well as in the E²PROM of the slave, the SAP5 **will not process a *Write_Extended_ID_Code_1* request** if the data sent does not match the data that is stored in protected part of the *ID_Code_Extension_1* register. It will neither access the E²PROM nor send a slave response in this case.

  Note: As defined in the AS-i Complete Specification [1] a modification of the A/B Slave selector bit must be performed bit selective. That means the AS-i Master must read the *ID_Code_Extension_1* first, modify Bit3 and send the new 4 bit word that consists of the modified Bit3 and the unmodified Bits 2…0 back to the slave.
- If the *Inhibit_Write_ID1* flag is **not** set ('0'), *ID_Code_Extension_1* is completely user configurable. The data to construct the slave response to a *Read_ID_Code_1* request is completely taken from the *ID_Code_Extension_1* register on E²PROM address 1 in the user area.

  A *Write_Extended_ID_Code_1* request will always be answered and initiate an E²PROM write access procedure in this case.

Manufacturer configuration of the *ID_Code_Extension_1* register is only possible as long as the *Lock_EE_PRG* flag is not yet set. In this case, the *Write_Extended_ID_Code_1* request causes a write access that differs from the procedure described on page 17. Instead of the *Security_Flag* procedure, the *ID_Code_Extension_1* is written to both E²PROM addresses 1 and 2 in the User Area of the E²PROM. This way of duplicate saving ensures data consistency even in the case of an accidental interruption of the E²PROM write process during modification of Bit3 in Extended Address Mode. Refer to Table 40 for an overview about the different programming and readout options of *ID_Code_Extension_1.*

Table 40: Write Protection of *ID_Code_Extension_1*

Master Call	*ID_Code*	*Lock_EE_PRG*	*Inhibit_Write_ID1*	Reaction	slave answer
WID1	≠ 0xA	0	0	Write *ID1_user* + *ID1_manufacturer* (user area address 1 and 2)	yes
			1	New ID1 matches *ID1_manufacturer*: write *ID1_user* + *ID1_manufacturer*	yes
				New ID1 does not match *ID1_manufacturer*: No action	no
		1	0	Write *ID1_user*	yes
			1	New ID1 matches *ID1_manufacturer*: Write *ID1_user*	yes
				New ID1 does not match *ID1_manufacturer*: No action	no
	0xA	0	0	Write *ID1_user* + *ID1_manufacturer*	yes
			1	New ID1[2:0] matches *ID1_manufacturer*[2:0]: write *ID1_user* + *ID1_manufacturer*	yes
				New ID1[2:0] does not match *ID1_manufacturer*[2:0]: No action	no
		1	0	Write *ID1_user*	yes
			1	New ID1[2:0] matches *ID1_manufacturer*[2:0]: write *ID1_user*	yes
				New ID1[2:0] does not match *ID1_manufacturer*[2:0]: No action	no
RID1	≠ 0xA	0	0	Return *ID1_user*	yes
			1	Return *ID1_manufacturer*	
		1	0	Return *ID1_user*	
			1	Return *ID1_manufacturer*	
	0xA	0	0	Return *ID1_user*	
			1	Return *ID1_user*[3], *ID1_manufacturer*[2:0]	
		1	0	Return *ID1_user*	
			1	Return *ID1_user*[3], *ID1_manufacturer*[2:0]	

The slave answer to a *Write_ID_Code1* request is ‘0’ in any case as specified in Table 6.

5 Application Circuits

The following figures show typical application cases of the SAP5. Please note that these schematics show only principle circuit drafts. For more detailed application information see the separate **SAP5 Application Notes** document.

Figure 14 outlines a standard slave application circuit compliant to the first AS-i IC.

Figure 15 shows an Safety Mode application circuit.

A Master Mode application is shown in Figure 16.

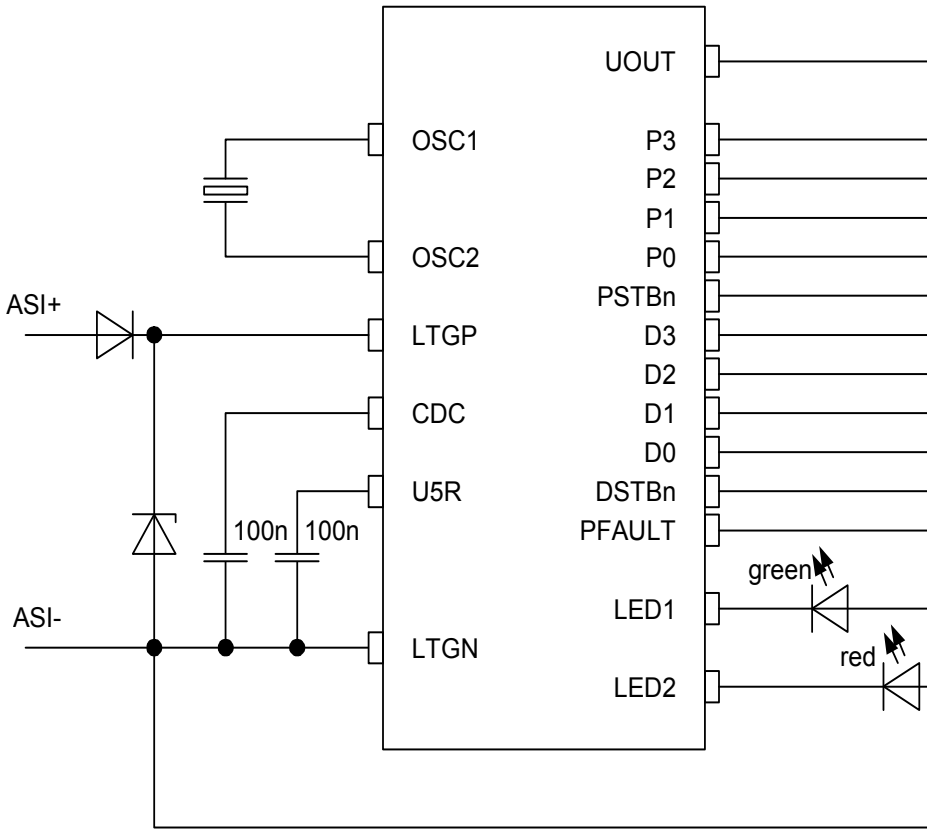


Figure 14: Standard Application circuit, direction of Data I/O depends on *IO_Cod*

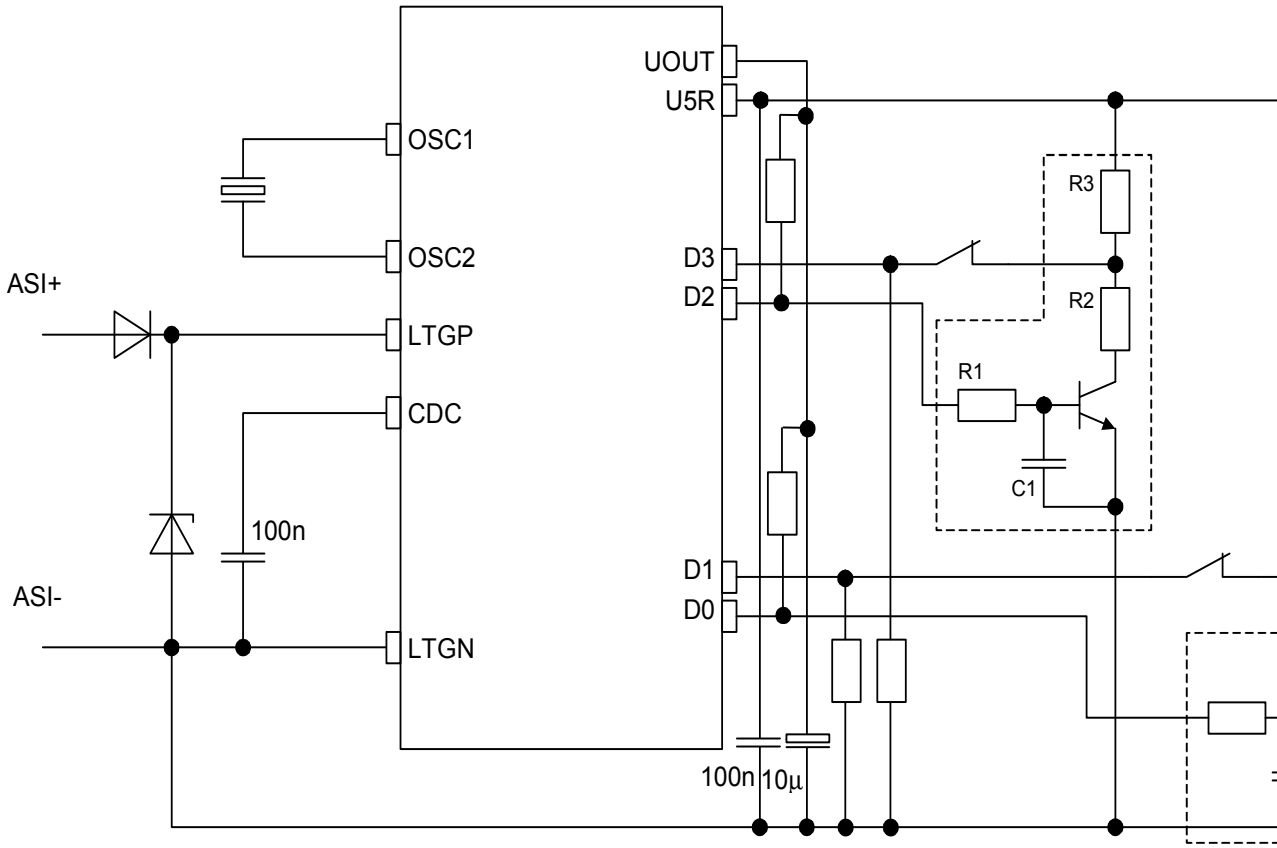


Figure 15: Safety Mode Application

R1 and C1 form a low-pass-filter for the delay of the output of the SAP5 IC for about 20 µs. The transistor performs the voltage divider R2/R3 shift the low level to 1.5V … 2.5V. The high level is provided from the pin's pull-up feature.

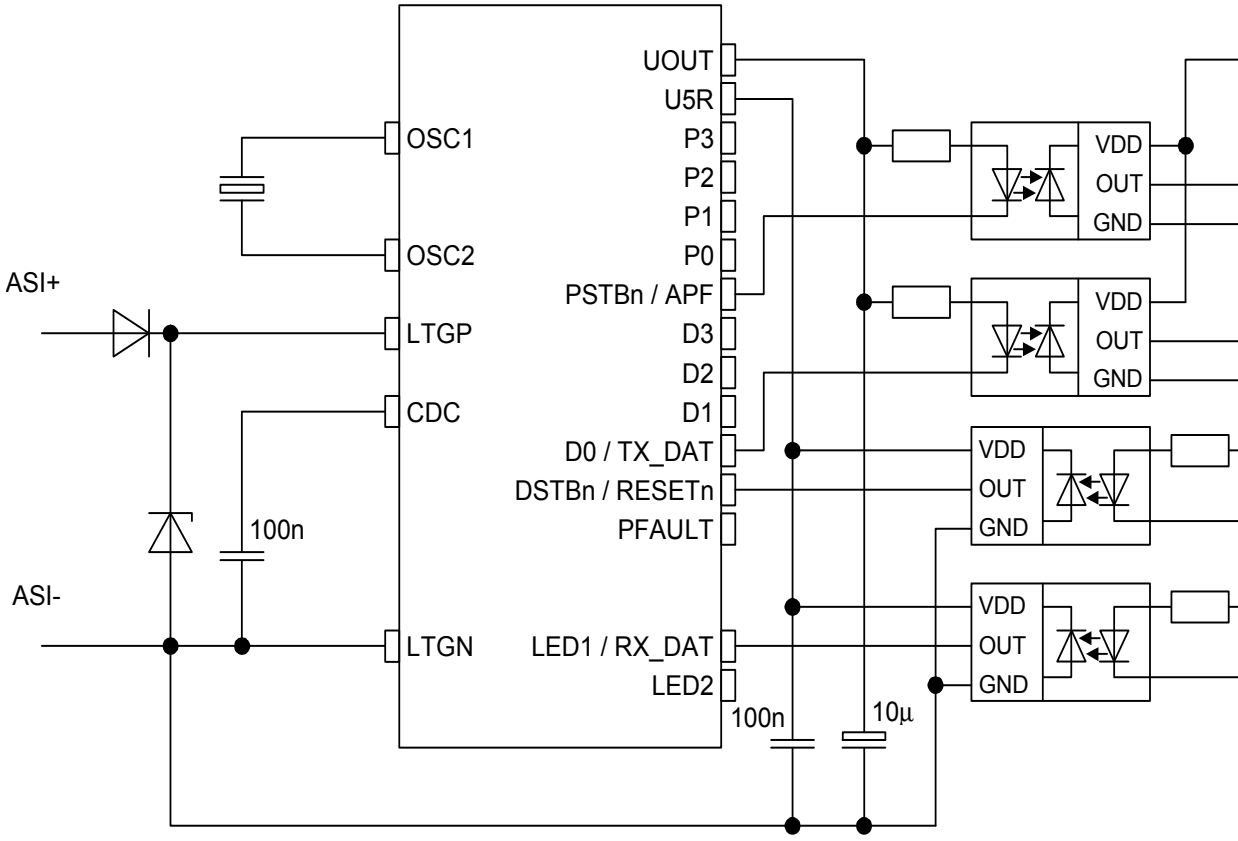
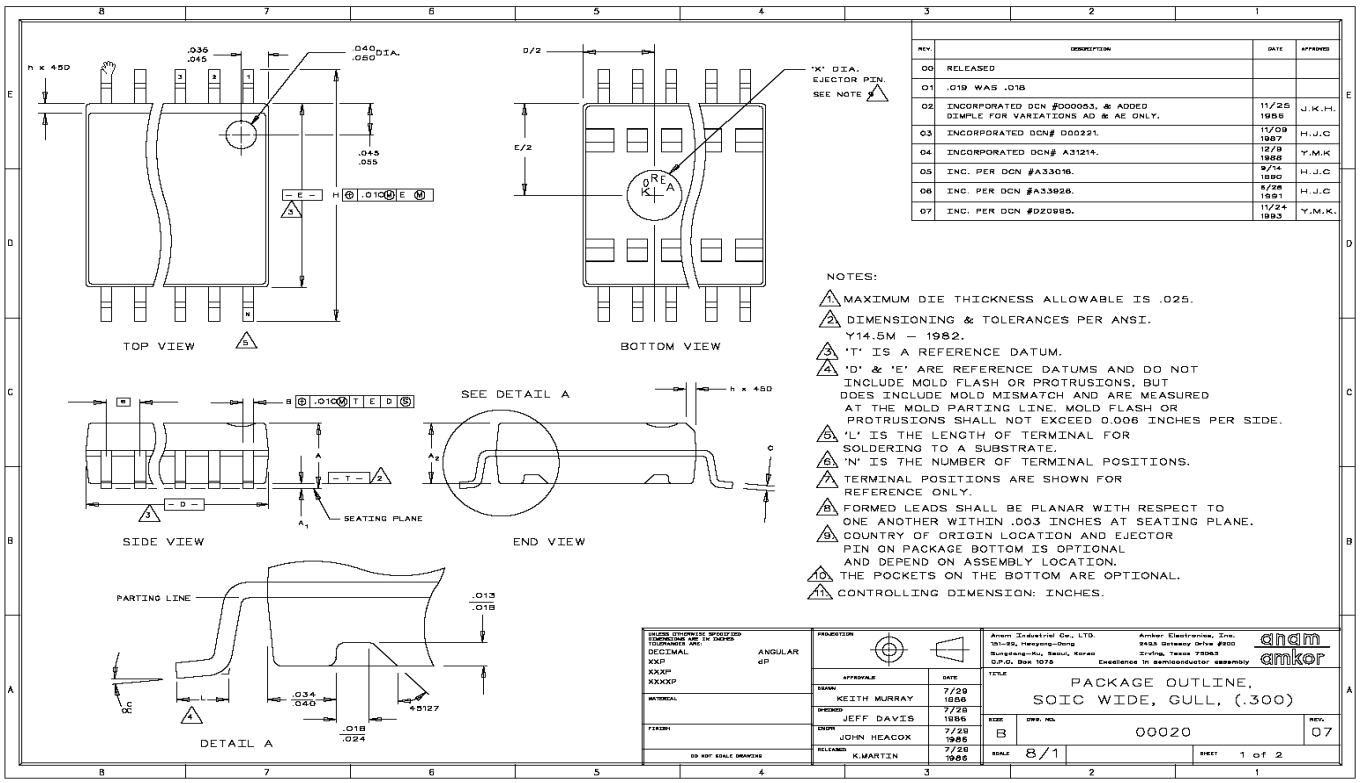


Figure 16: SAP5 Master Mode Application

6 Package Outlines

The IC is packaged in a 20 pin SOP20-300mil package (Figure 17) or in a 16 pin SOP16-300mil package (Figure 17).



THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	NOTE VARIATIONS	3 D MIN.	NOM.	MAX.	5 N
A	.097	.101	.104		AA	.402	.407	.412	16
A_1	.0050	.009	.0115		AB	.451	.456	.461	18
A_2	.090	.092	.094		AC	.500	.505	.510	20
B	.014	.016	.019		AD	.602	.607	.612	24
C	.0091	.010	.0125		AE	.701	.706	.711	28
D	SEE VARIATIONS			3					
E	.292	.296	.299						
e	.050 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			5					
∝	0D	5D	8D						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	NOTE VARIATIONS	3 D MIN.	NOM.	MAX.	5 N
A	2.46	2.56	2.64		AA	10.21	10.34	10.46	16
A_1	0.127	0.22	0.29		AB	11.46	11.58	11.71	18
A_2	2.29	2.34	2.39		AC	12.70	12.83	12.95	20
B	0.35	0.41	0.48		AD	15.29	15.42	15.54	24
C	0.23	0.25	0.32		AE	17.81	17.93	18.06	28
D	SEE VARIATIONS			3					
E	7.42	7.52	7.59						
e	1.27 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			5					
∝	0D	5D	8D						
X	2.16	2.36	2.54						

Figure 17: Package Drawings and Dimensions for the SOP16/SOP20-300mil versions

7 Package Marking

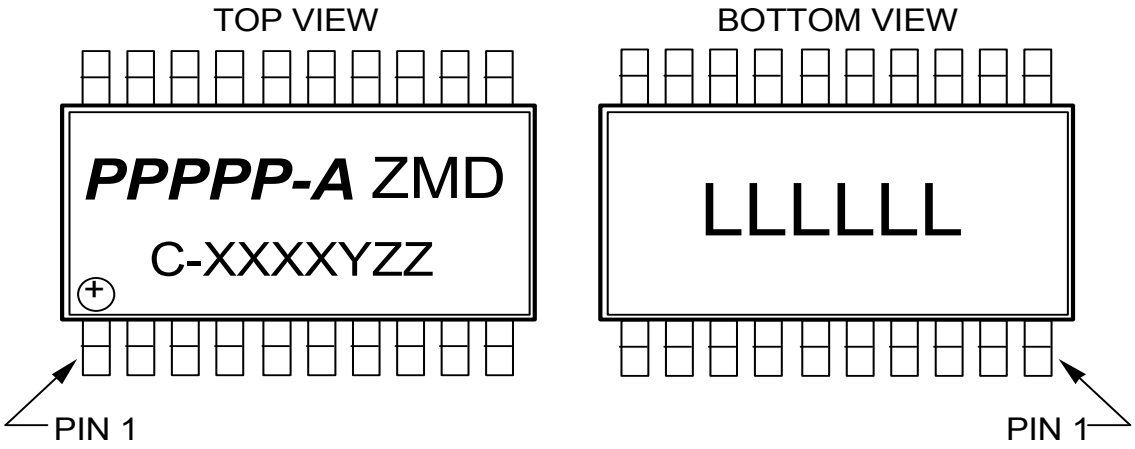


Figure 18: Package Marking 20 pin version

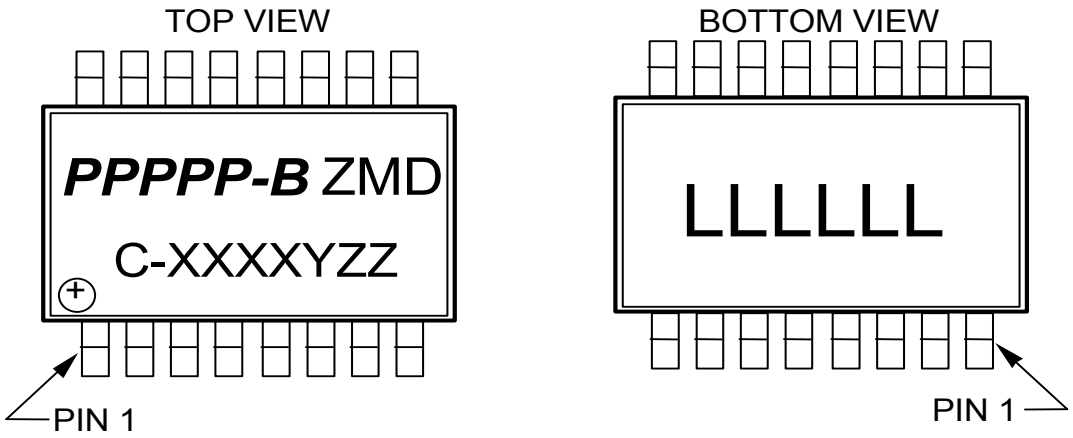


Figure 19: Package Marking 16 pin version

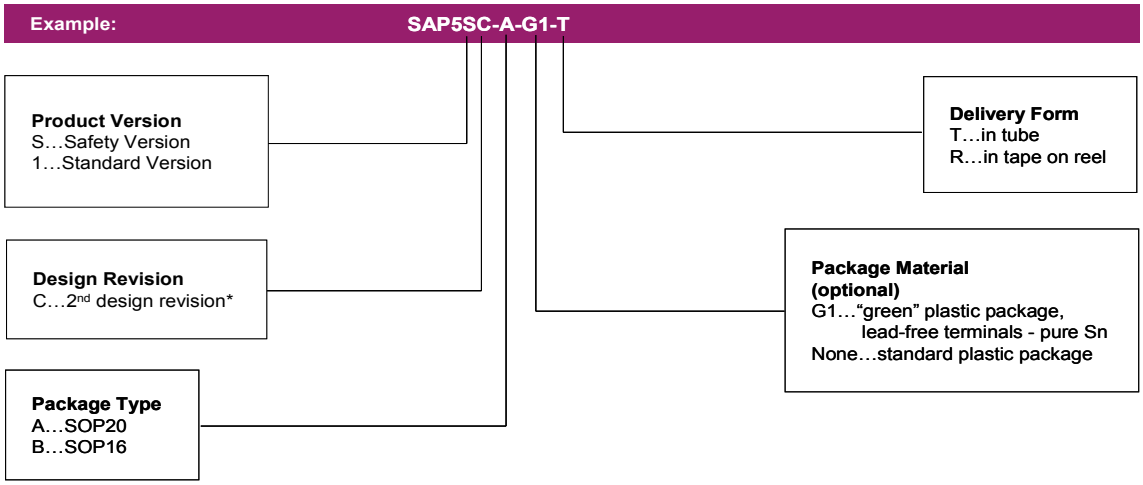
Top Marking:	PPPPP-A	Product name SOP20 Package
	PPPPP-B	Product name SOP16 Package
	ZMD	Manufacturer
	C-	Revision code
	XXXX	Date code (year and week)
	Y	Assembly location
	ZZ	Traceability
Bottom Marking:	LLLLLL	ZMD Lot Number

8 Ordering Information

Ordering Code	Description	Operating Temperature Range	Package Type	Device Marking	Shipping Form
SAP5SC-A-G1-T	full Safety-Mode)[1]	-25°C to 85°C	20-pin SOP		Tubes (37 parts/tube)
SAP5SC-A-G1-R	full Safety-Mode)[1]	-25°C to 85°C	20-pin SOP		Tape-and-Reel (1000 parts/reel)
SAP5SC-B-G1-T	full Safety-Mode)[1]	-25°C to 85°C	16-pin SOP		Tubes (46 parts/tube)
SAP5SC-B-G1-R	full Safety-Mode)[1]	-25°C to 85°C	16-pin SOP		Tape-and-Reel (1000 parts/reel)
SAP51C-A-G1-T	without Safety-Mode)[2]	-25°C to 85°C	20-pin SOP		Tubes (37 parts/tube)
SAP51C-A-G1-R	without Safety-Mode)[2]	-25°C to 85°C	20-pin SOP		Tape-and-Reel (1000 parts/reel)
SAP51C-B-G1-T	without Safety-Mode)[2]	-25°C to 85°C	16-pin SOP		Tubes (46 parts/tube)
SAP51C-B-G1-R	without Safety-Mode)[2]	-25°C to 85°C	16-pin SOP		Tape-and-Reel (1000 parts/reel)

)[1] Full featured SAP5 IC, no IC functions were blocked by E²PROM programming. IC is user programmable to operation in Slave Mode, Master Mode and Safety Mode

)[2] SAP5 IC with functional compliance to SAP4.1 IC + features according to AS-i Complete Spec v3.0
AS-I Safety option is disabled by an E²PROM flag that is not accessible for the user.



* Current design revision; other design revisions are currently not available.

Not all product versions are available - please see the next page or ask ZMD for the required ones.

For the current revision of this document and for additional product information please look at www.zmd.biz..

9 Contact Information

9.1 ZMD Sales Contacts

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Please also see www.zmd.biz for most current information on ZMD AS-Interface products and technical product support.

9.2 ZMD Distribution Partners

ZMD partners with WBC for device distribution in Europe and Future Electronics / All American for North- and South America.

Germany/EMEA	
AVNET Memec Im Technologiepark 2-8 D-85586 Poing Phone: +49 8121 775 155 Fax: +49 8121 775 592 E-mail: poing@avnet-memec.com Internet: http://www.avnet-memec.com/	Other local AVNET Memec representatives on http://www.avnet-memec.com/. Other ZMD representatives on www.zmd.biz.

Germany	***Canada, North/SouthAmerica***	***North America***
Henskes Electronic Components GmbH Bremer Straße 7 D-30880 Laatzen (Rethen) Phone: +49 5102 938117 Fax: +49 5102 938198 E-mail: hg.senf@henskes.com Internet: www.henskes.de	Future Electronics Worldwide Corporate Headquarters 237 Hymus blvd. Pointe-Claire, Quebec, H9R 5C7 Phone: +1 (514) 694-7710 Fax: +1 (514) 695-3707 Internet: www.futureelectronics.com	All American Semiconductor Inc. 230Devcon Drive San Jose CA 95112 Phone: +1 (800) 573-ASAP Fax: +48 (0) 71 788 80 13 Internet: www.allamerican.com

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Internix Inc. 59-10Takakura-cho Hachioji Tokyo 192-0033 Phone.: +81 426 44 8786 Fax: +81 426 48 5204 E-mail: hisozaki@internix.co.jp Internet:www.internix.co.jp/	Tempe technologies 62 Oude Kaap Estate Dowerglen, South Africa Phone: +27 11 4520530 Fax: +27 11 4520543 Internet: www.tempetech.co.za	M/s Excel Eltech India PVT Ltd. # 77 J S Tower, 11 FLOOR Opp St Patricks Church Brigade Road Bangalore - 560 025 Phone: +91 80 2 557 3582 Fax: +91 80 2 557 3609 E-mail: sales@exceleltechindia.com

9.3 AS-International Association

Documentation and promotional materials as well as detailed technical specifications regarding the AS-Interface Bus Standard are available from:

AS-International Association:	Contact - Rolf Becker Zum Taubengarten 52 D-63571 Gelnhausen PO Box 1103 Zip (63551) Phone: +49 6051 47 32 12 Fax: +49 6051 4732 82 E-mail: info@as-interface.net Internet: www.as-interface.net

Refer to www.as-interface.net for contact information on local AS-Interface associations which provide special support within Europe, in the US and in Japan.

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