

Brief Description

The ZSPM1035A is a flexible true-digital single-phase PWM controller optimally configured for use with the Murata Power Solutions 35A Power Block OKLP-X/35-W12-C in smart digital power solutions.

The ZSPM1035A integrates a digital control loop, optimized for maximum flexibility and stability, as well as load step and steady-state performance. In addition, a rich set of protection and monitoring functions is provided. On-chip, non-volatile memory (NVM) and an I²C™ interface facilitate configuration.

IDT's PC-based Pink Power Designer™ graphic user interface (GUI) provides a user-friendly and easy-to-use interface to the ZSPM1035A for communication, monitoring, and configuration of the protection and sequencing features.

A downloadable reference solution is available, including a graphical user interface, layout guidelines, bill of materials, and step-by-step instructions.

Features

- Programmable digital control loop
- Advanced digital control techniques
 - Tru-sample Technology™
 - State-Law Control™ (SLC)
 - Sub-cycle Response™ (SCR)
- Improved transient response and noise immunity
- Protection features
 - Over-current protection
 - Over-voltage protection (VIN, VOUT)
 - Under-voltage protection (VIN, VOUT)
 - Overloaded startup
 - Continuous retry (“hiccup”) mode for fault conditions
- Fuse-based NVM for improved reliability
- Operation from a single 5V or 3.3V supply
- Optional PMBus™ address selection without external resistors

Benefits

- Fast time-to-market using off-the-shelf, optimally configured controller and power block
- Fast configurability and design flexibility
- Simplified design flow and high reliability via proven system design solution
- Reduced component count through system level integration
- Simplified monitoring for system power and thermal management
- Pin-to-pin compatible with the ZSPM1035C and ZSPM1035D PWM controllers enabling point-of-load platform designs with or without digital communication
- Higher energy efficiency across all output loading conditions

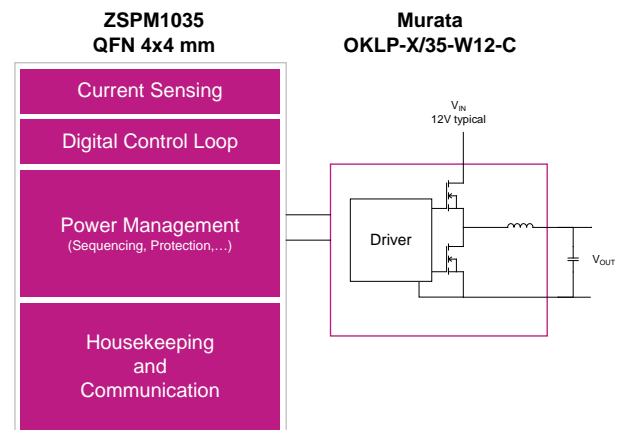
Available Support

- Evaluation Kit
- Reference Solution
- PC-based Pink Power Designer™ GUI

Physical Characteristics

- Operation temperature: -40°C to +125°C
- V_{OUT}: 0.35V to 3.6V
- Lead free (RoHS compliant) 24-pin QFN package (4mm x 4mm)

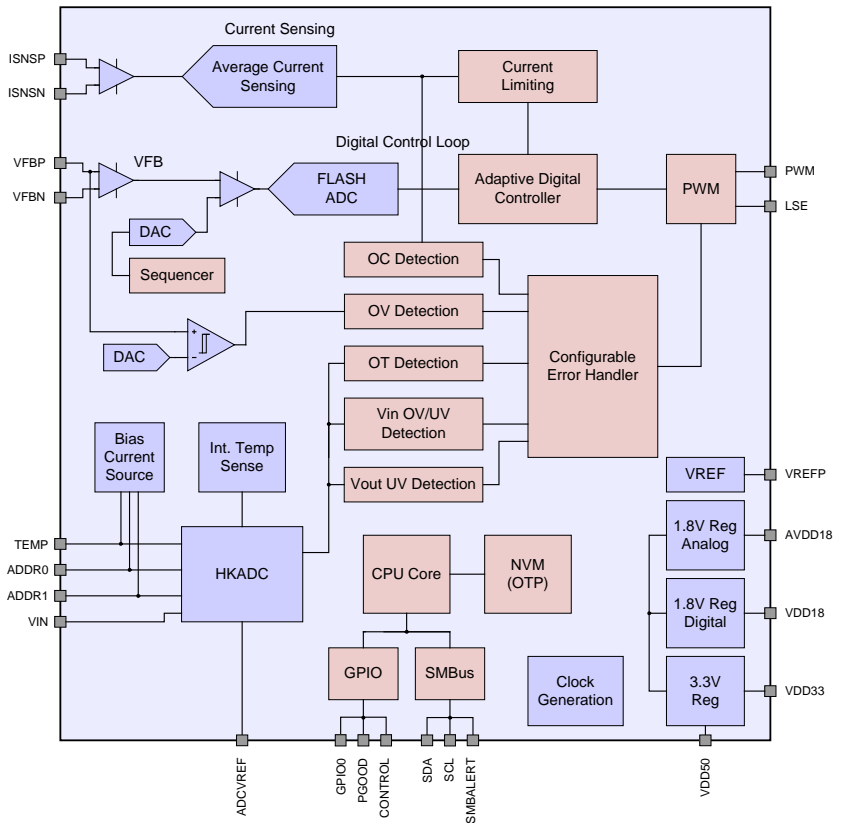
ZSPM1035A Typical Application Diagram



* I²C™ is a registered trademark of NXP.

ZSPM1035A Block Diagram

- Typical Applications**
- ❖ Telecom Switches
 - ❖ Servers and Storage
 - ❖ Base Stations
 - ❖ Network Routers
 - ❖ Industrial Applications
 - ❖ Single-Rail/Single-Phase Supplies for Processors, ASICs, FPGAs, DSPs



Ordering Information

| Sales Code | Description | Package |
|----------------|---|---------|
| ZSPM1035AA1W 1 | ZSPM1035A Lead-free QFN24 — Temperature range: -40°C to +125°C * | Reel |
| ZSPM8035-KIT | Evaluation Kit for ZSPM1035A with PMBus™ Communication Interface — Pink Power Designer™ GUI for kit can be downloaded from the IDT web site at www.IDT.com/ZSPM1035A | Kit |

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1 IC Characteristics

Note: The absolute maximum ratings are stress ratings only. The ZSPM1035A might not function or be operable above the recommended operating conditions. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. IDT does not recommend designing to the “Absolute Maximum Ratings.”

1.1. Absolute Maximum Ratings

| PARAMETER | PINS | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------------|---|------------------|------|-----|------|-------|
| Supply voltages | | | | | | |
| 5V supply voltage | VDD50 | dV/dt < 0.15V/μs | -0.3 | | 5.5 | V |
| Maximum slew rate | | | | | 0.15 | V/μs |
| 3.3V supply voltage | VDD33 | | -0.3 | | 3.6 | V |
| 1.8V supply voltage | VDD18 AVDD18 | | -0.3 | | 2.0 | V |
| Digital pins | | | | | | |
| Digital I/O pins | SCL SDA SMBALERT GPIO0 CONTROL PGOOD LSE PWM | | -0.3 | | 5.5 | V |
| Analog pins | | | | | | |
| Current sensing | ISNSP, ISNSN | | -0.3 | | 5.5 | V |
| Voltage feedback | VFBN VFBN | | -0.3 | | 2.0 | V |
| All other analog pins | ADCVREF VREFP TEMP VIN ADDR0 ADDR1 | | -0.3 | | 2.0 | V |
| Ambient conditions | | | | | | |
| Storage temperature T _{STOR} | | | -40 | | 150 | °C |

1.2. Recommended Operating Conditions

| PARAMETER | Symbol | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------|------------|-----|-----|-----|-------|
| Ambient operation temperature | T_{AMB} | | -40 | | 125 | °C |
| Thermal resistance junction to ambient | θ_{JA} | | | 40 | | K/W |

1.3. Electrical Parameters

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------------------------|--|------|------|-------|-------|
| Supply voltages | | | | | | |
| 5V supply voltage —VDD50 pin | V_{VDD50} | | 4.75 | 5.0 | 5.25 | V |
| 5V supply current | I_{VDD50} | VDD50=5.0V | | 23 | | mA |
| 3.3V supply voltage | V_{VDD33} | Supply for both the VDD33 and VDD50 pins if the internal 3.3V regulator is not used. | 3.0 | 3.3 | 3.6 | V |
| 3.3V supply current | I_{VDD33} | VDD50=VDD33=3.3V | | 23 | | mA |
| Internally generated supply voltages | | | | | | |
| 3.3V supply voltage—VDD33 pin | V_{VDD33} | VDD50=5.0V | 3.0 | 3.3 | 3.6 | V |
| 3.3V output current | I_{VDD33} | VDD50=5.0V | | | 2.0 | mA |
| 1.8V supply voltages—AVDD18 and VDD18 pins | V_{AVDD18} V_{VDD18} | VDD50=5.0V | 1.72 | 1.80 | 1.98 | V |
| 1.8V output current | | | | | 0 | mA |
| Power on reset (POR) threshold for VDD33 pin – on | $V_{TH_POR_ON}$ | | | 2.8 | | V |
| Power on reset threshold for VDD33 pin – off | $V_{TH_POR_OFF}$ | | | 2.6 | | V |
| Digital IO pins (GPIO0, CONTROL, PGOOD) | | | | | | |
| Input high voltage | | VDD33=3.3V | 2.0 | | | V |
| Input low voltage | | VDD33=3.3V | | | 0.8 | V |
| Output high voltage | | VDD33=3.3V | 2.4 | | VDD33 | V |
| Output low voltage | | | | | 0.5 | V |
| Input leakage current | | | | | ±1.0 | μA |
| Output current – high | | | | | 2.0 | mA |
| Output current – low | | | | | 2.0 | mA |
| Digital IO pins with tri-state capability (LSE, PWM) | | | | | | |
| Output high voltage | | VDD33=3.3V | 2.4 | | VDD33 | V |
| Output low voltage | | | | | 0.5 | V |
| Output current – high | | | | | 2.0 | mA |

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------|------------|-----|-----|------|-------|
| Output current – low | | | | | 2.0 | mA |
| Tri-state leakage current | | | | | ±1.0 | µA |
| SMBus pins (SCL, SDA, SMBALERT) – open drain | | | | | | |
| Input high voltage | | VDD33=3.3V | 2.0 | | | V |
| Input low voltage | | VDD33=3.3V | | | 0.8 | V |
| Maximum bus voltage | | | | | 5.25 | V |
| Output current – low | | | | | 2.0 | mA |
| Output voltage* | | | | | | |
| Set-point voltage | | | 0 | | 1.4 | V |
| Set-point resolution | | | | 1.4 | | mV |
| Set-point accuracy | | VOUT=1.2V | | 1 | | % |
| *Without external voltage divider (see section 3.3.2) | | | | | | |
| Inductor current measurement | | | | | | |
| Common mode voltage — ISNSP and ISNSN pins relative to AGND | | | 0 | | 5.0 | V |
| Differential voltage range across ISNSP and ISNSN pins | | | | | ±100 | mV |
| Accuracy | | | | 5 | | % |
| Recommended DCR sense voltage for maximum output current | | | 10 | | | mV |
| Digital pulse width modulator | | | | | | |
| Switching frequency | f _{sw} | | | 500 | | kHz |
| Resolution | | | | 163 | | ps |
| Frequency accuracy | | | | 2.0 | | % |
| Over-voltage protection | | | | | | |
| Reference DAC | | | | | | |
| Set-point voltage | | | 0 | | 1.58 | V |
| Resolution | | | | 25 | | mV |
| Set point accuracy | | | | 2 | | % |
| Comparator | | | | | | |
| Hysteresis | | | | 35 | | mV |
| Housekeeping analog-to-digital converter (HKADC) input pins | | | | | | |
| Input voltage—TEMP, VIN, ADDR0, and ADDR1 pins | | | 0 | | 1.44 | V |
| Source impedance Vin sensing | | | | | 3 | kΩ |

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------|------------|-----|------|-----|-------|
| ADC resolution | | | | 0.7 | | mV |
| External temperature measurement ** | | | | | | |
| Bias currents for external temperature sensing —TEMP pin | | | | 60 | | μA |
| Resolution—TEMP pin | | | | 0.16 | | K |
| Accuracy of measurement—TEMP pin | | | | ±5.0 | | K |
| ** Supported sense elements: PN-junction | | | | | | |
| Internal temperature measurement | | | | | | |
| Resolution | | | | 0.22 | | K |
| Accuracy of measurement | | | | ±5.0 | | K |

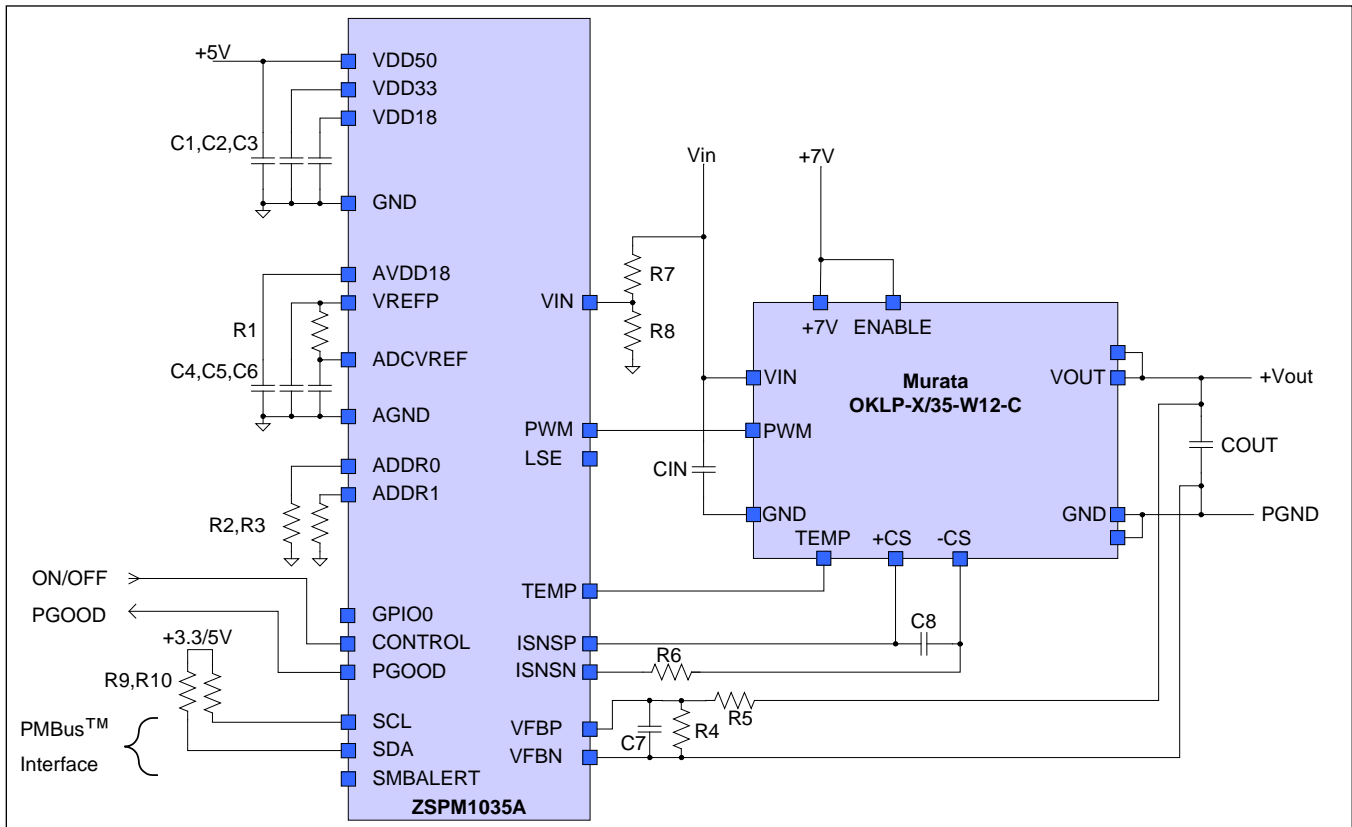
2 Product Summary

2.1. Overview

The ZSPM1035A is a flexible true-digital single-phase PWM controller optimally configured for use with the Murata Power Solutions 35A Power Block OKLP-X/35-W12-C in smart digital power solutions. It offers a PMBus™-configurable digital power control loop, incorporating output voltage sensing and average inductor current sensing, bundled with extensive fault monitoring and handling options.

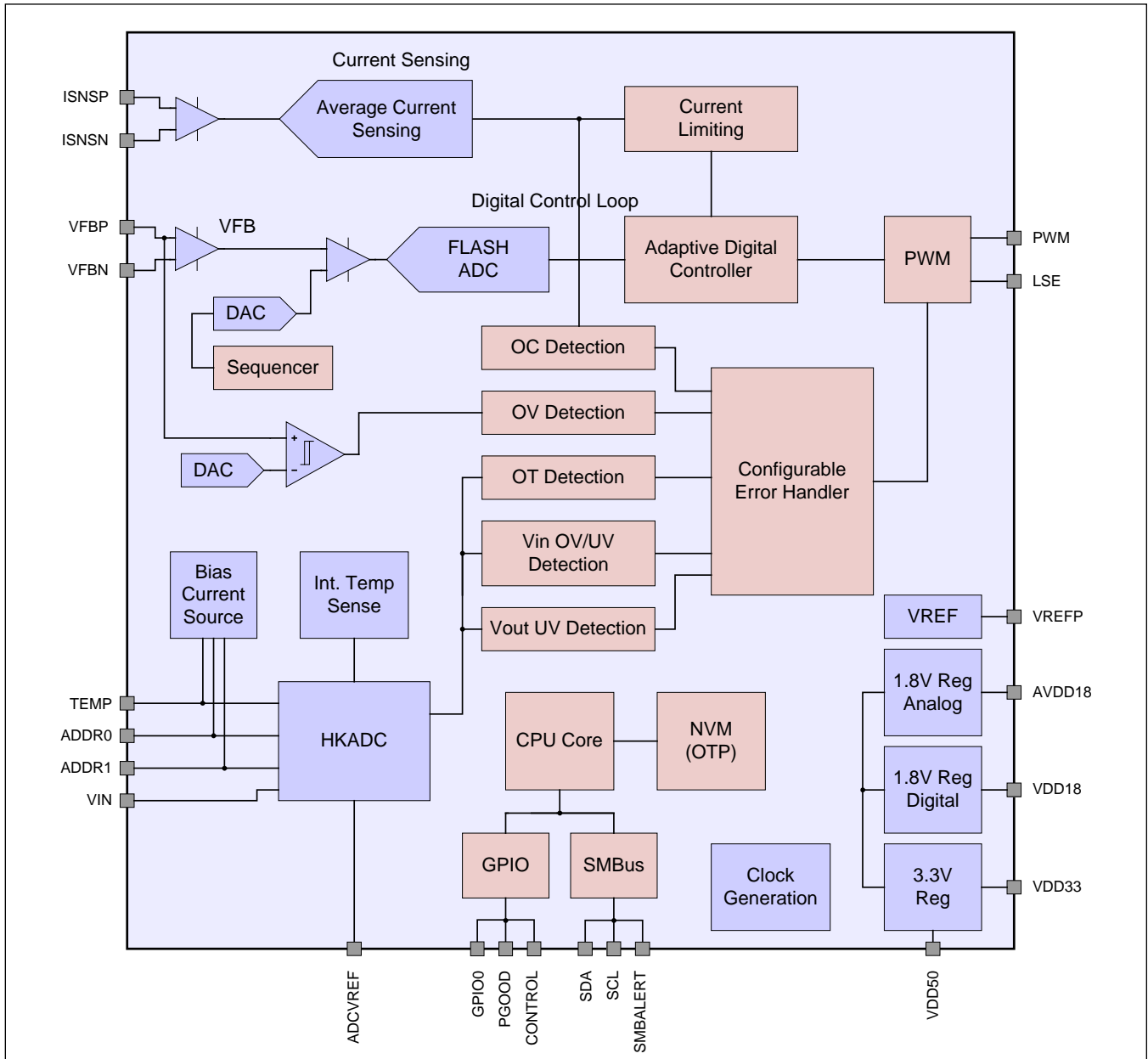
Several different functional units are integrated in the device. A dedicated digital control loop is used to provide fast loop response and optimal output voltage regulation. This includes output voltage sensing, average inductor current sensing, a digital control law, and a digital pulse-width modulator (DPWM). In parallel, a dedicated, configurable error handler allows for fast and flexible detection of error signals and their appropriate handling. A housekeeping analog-to-digital converter (HKADC) ensures the reliable and efficient measurement of environmental signals, such as input voltage and temperature. An application-specific, low-energy integrated microcontroller is used to control the overall system. Among other things, it manages configuration of the various logic units and handles the PMBus™ communication protocol. A PMBus™/SMBus/I²C™ interface is incorporated to connect with the outside world; supported by control and power-good signals.

Figure 2.1 Typical Application Circuit with a 5V Supply Voltage



A high-reliability, high-temperature one-time programmable memory (OTP) is used to store configuration parameters. All required bias and reference voltages are internally derived from the external supply voltage.

Figure 2.2 Block Diagram



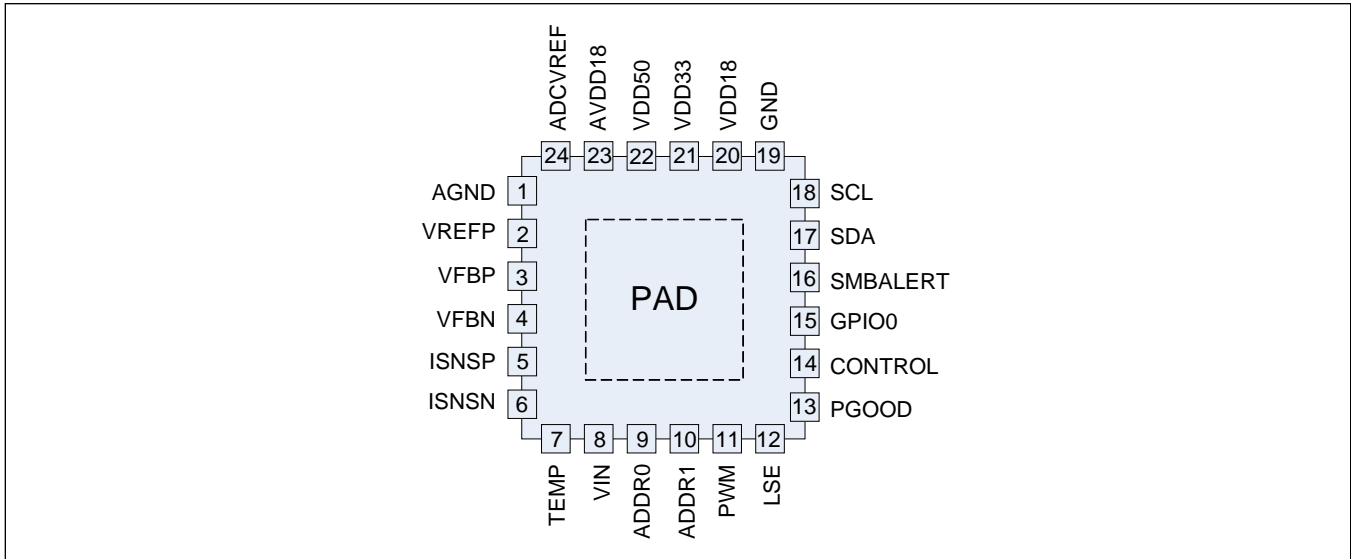
2.2. Pin Description

| Pin | Name | Direction | Type | Description |
|-----|----------|--------------|---------|---|
| 1 | AGND | Input | Supply | Analog Ground |
| 2 | VREFP | Output | Supply | Reference Terminal |
| 3 | VFBP | Input | Analog | Positive Input of Differential Feedback Voltage Sensing |
| 4 | VFBN | Input | Analog | Negative Input of Differential Feedback Voltage Sensing |
| 5 | ISNSP | Input | Analog | Positive Input of Differential Current Sensing |
| 6 | ISNSN | Input | Analog | Negative Input of Differential Current Sensing |
| 7 | TEMP | Input | Analog | Connection to External Temperature Sensing Element |
| 8 | VIN | Input | Analog | Power Supply Input Voltage Sensing |
| 9 | ADDR0 | Input | Analog | SMBus Address Selection 0 |
| 10 | ADDR1 | Input | Analog | SMBus Address Selection 1 |
| 11 | PWM | Output | Digital | High-side FET Control Signal |
| 12 | LSE | Output | Digital | Low-side FET Control Signal |
| 13 | PGOOD | Output | Digital | PGOOD Output (Internal Pull-Down) |
| 14 | CONTROL | Input | Digital | Control Input |
| 15 | GPIO0 | Input/Output | Digital | General Purpose Input/Output Pin |
| 16 | SMBALERT | Output | PMBus™ | SMBus Alert Output |
| 17 | SDA | Input/Output | PMBus™ | SMBus Shift Data I/O |
| 18 | SCL | Input | PMBus™ | SMBus Shift Clock Input (Slave-only) |
| 19 | GND | Input | Supply | Digital Ground |
| 20 | VDD18 | Output | Supply | Internal 1.8V Digital Supply Terminal |
| 21 | VDD33 | Input/Output | Supply | 3.3V Supply Voltage Terminal |
| 22 | VDD50 | Input | Supply | 5.0V Supply Voltage Terminal |
| 23 | AVDD18 | Output | Supply | Internal 1.8V Analog Supply Terminal |
| 24 | ADCVREF | Input | Analog | Analog-to-Digital Converter (ADC) Reference Terminal |
| PAD | PAD | Input | Supply | Exposed PAD, Digital Ground |

2.3. Available Packages

The ZSPM1035A is available in a 24-pin QFN package. The pin-out is shown in Figure 2.3. The mechanical drawing of the package can be found in Figure 6.1.

Figure 2.3 Pin-Out QFN24 Package



3 Functional Description

3.1. Power Supply Circuitry, Reference Decoupling, and Grounding

The ZSPM1035A incorporates several internal power regulators in order to derive all required supply and bias voltages from a single external supply voltage. This supply voltage can be either 5V or 3.3V depending on whether the internal 3.3V regulator should be used. If the internal 3.3V regulator is not used, 3.3V must be supplied to the 3.3V and 5V supply pins. Decoupling capacitors are required at the VDD33, VDD18, and AVDD18 pins (1.0 μ F minimum; 4.7 μ F recommended). If the 5.0V supply voltage is used, i.e. the internal 3.3V regulator is used, a small load current can be drawn from the VDD33 pin. This can be used to supply pull-up resistors, for example.

The reference voltages required for the analog-to-digital converters are generated within the ZSPM1035A. External decoupling must be provided between the VREFP and ADCVREF pins. Therefore, a 4.7 μ F capacitor is required at the VREFP pin and a 100nF capacitor is required at the ADCVREF pin. The two pins should be connected with approximately 50 Ω resistance in order to provide sufficient decoupling between the pins.

Three different ground connections (the pad, AGND pin, and GND pin) are available on the outside of the package. These should be connected together to a single ground tie. A differentiation between analog and digital ground is not required.

3.2. Reset/Start-up Behavior

The ZSPM1035A employs an internal power-on-reset (POR) circuit to ensure proper start up and shut down with a changing supply voltage. Once the supply voltage increases above the POR threshold voltage, the ZSPM1035A begins the internal start-up process. Upon its completion, the device is ready for operation.

3.3. Digital Power Control

3.3.1. Overview

The digital power control loop consists of the integral parts required for the control functionality of the ZSPM1035A. A high-speed analog front-end is used to digitize the output voltage. A digital control core uses the acquired information to provide duty-cycle information to the PWM, which controls the drive signals to the power stage.

3.3.2. Output Voltage Feedback

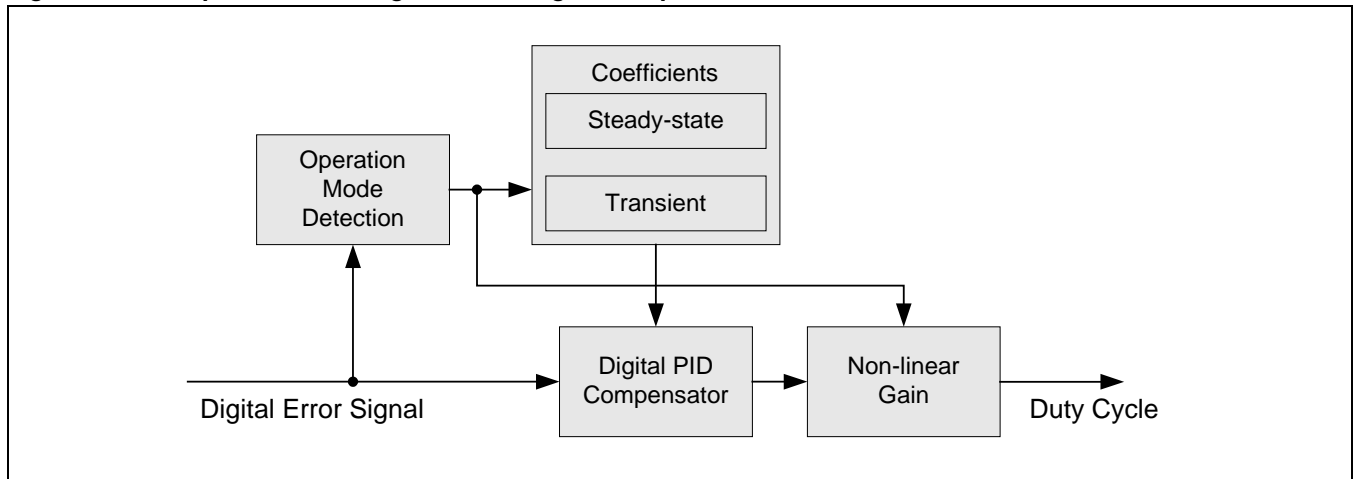
The voltage feedback signal is sampled with a high-speed analog front-end. The feedback voltage is differentially measured and subtracted from the voltage reference provided by a reference digital-to-analog converter (DAC) using an error amplifier. A flash ADC is then used to convert the voltage into its digital equivalent. This is followed by internal digital filtering to improve the system's noise rejection.

An external feedback divider is required for output voltages above 1.20V. The reference DAC generates a voltage up to 1.44V. Keeping the voltage on the feedback pin (VFBP) below 1.20V guarantees sufficient headroom for the output voltage compensation loop.

3.3.3. Digital Compensator

The sampled output voltage is processed by a digital control loop in order to modulate the DPWM output signals controlling the power stage. This digital control loop works as a voltage-mode controller using a PID-type compensation. The basic structure of the controller is shown in Figure 3.1. The proprietary State-Law™ Control (SLC) concept features two parallel compensators, steady-state operation, and fast transient operation. The ZSPM1035A implements fast, reliable switching between the different compensation modes in order to ensure good transient performance and quiet steady state. This allows tuning the compensators individually for the respective needs; i.e. quiet steady-state and fast transient performance.

Figure 3.1 Simplified Block Diagram of the Digital Compensation



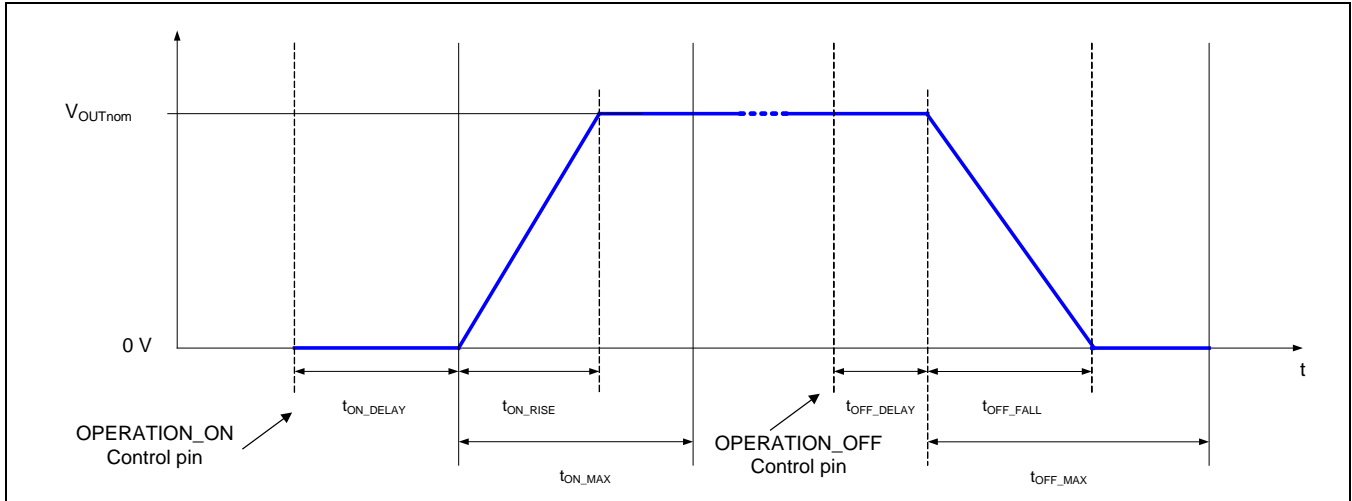
Three additional techniques are used to improve transient performance further.

- Tru-sample Technology™ is used to acquire fast, accurate, and continuous information about the output voltage so that the device can react quickly to any change in output voltage. Tru-sample Technology™ reduces phase-lag caused by sampling delays, reduces noise sensitivity, and improves transient performance.
- The Sub-cycle Response™ (SCR) technique, a method to drive the DPWM asynchronously during load transients, allows limiting the maximum deviation of the output voltage and recharging the output capacitors faster.
- A non-linear gain adjustment is used during large load transients to boost the loop gain and reduce the settling time.

3.3.4. Power Sequencing and the CONTROL Pin

The ZSPM1035A supports power-sequencing features including programmable ramp up/down and delays. The typical sequence of events is shown in Figure 3.2 and follows the PMBus™ standard. The individual values can be set using the appropriate configuration setting, which can be selected using the Pink Power Designer™ GUI. Three different configuration options are supported to turn the device on. The device can be configured to turn on immediately after POR, on an OPERATION_ON command, or on an edge on the CONTROL pin.

Figure 3.2 Power Sequencing

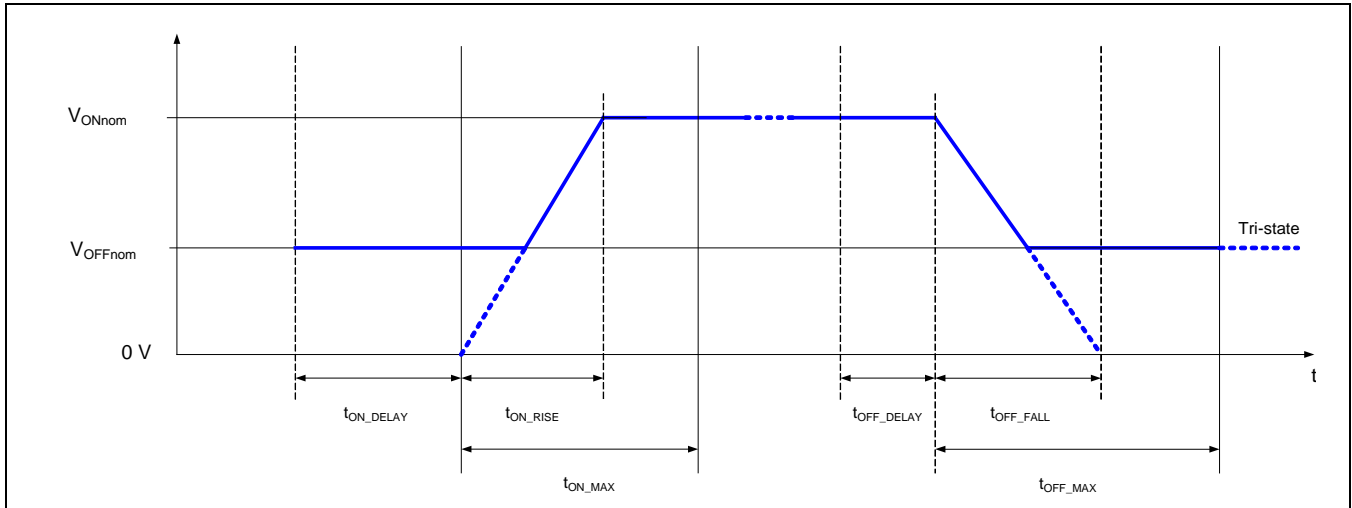


3.3.5. Pre-biased Start-up and Soft Stop

Dedicated pre-biased start-up logic ensures proper start-up of the power converter when the output capacitors are pre-charged to a non-zero output voltage. Closed-loop stability is ensured during this phase.

The ZSPM1035A also supports pre-biased off, i.e. the output voltage is not ramped down to zero and instead remains at a predefined level (V_{OFF_nom}). This value can be configured via the Pink Power Designer™. After receiving the shutdown command via the PMBus™ or the CONTROL pin, the ZSPM1035A ramps down the output voltage value to the predefined value. Once the value is reached, the PWM output will be put into tri-state mode in order to put the output driver into its tri-state mode.

Figure 3.3 Power Sequencing with Non-zero Off Voltage

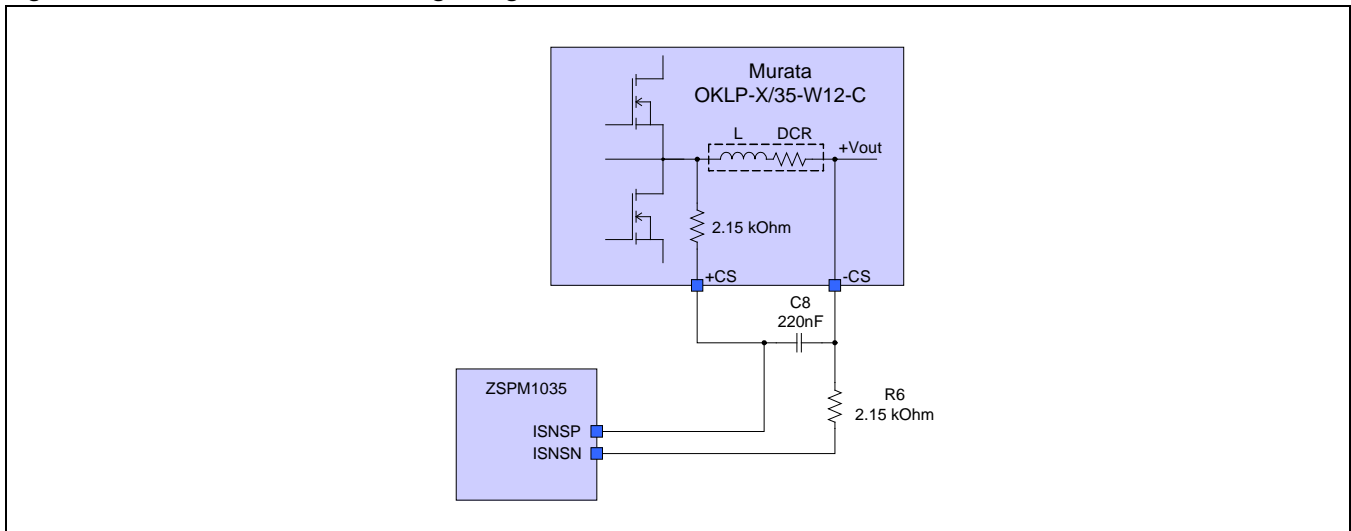


3.3.6. Current Sensing

The ZSPM1035A offers cycle-by-cycle average current sensing with configurable over-current protection. A dedicated ADC is used to provide fast and accurate current information over the switching period. The acquired information is compared with configurable current thresholds to report warning and error levels to the user. DCR current sensing across the inductor on the OKLP-X/25-W12-C power block is supported. Additionally, the device uses DCR temperature compensation via the external temperature-sensing element. This increases the accuracy of the current sense method by counteracting the significant change of the DCR over temperature.

To acquire accurate current information, the selection of the current-sensing circuit is of critical importance. The schematic of the required current-sensing circuitry is shown in Figure 3.4 for the widely used DCR current-sensing method, which uses the parasitic resistance of the inductor to acquire the current information. The principle is based on a matched time-constant between the inductor and the low-pass filter built from a 2.15kΩ resistor mounted on the Murata Power Block and C8. Resistor R6 should be a precision 2.15kΩ resistor in order to provide good DC voltage rejection, .i.e. reduce the influence of the output voltage level in the current measurement.

Figure 3.4 Inductor Current Sensing Using the DCR Method



End-of-line calibration is supported so that the ZSPM1035A can achieve improved accuracy over the full output current range. The full calibration method is detailed in the *ZSPM10xx Application Note—Programming and Calibration*. This allows the user to correct mismatches between the nominal DCR value used to configure the device and the actual DCR value in the application caused by effects such as manufacturing variations. The calibration range is limited to +/- 50% of the nominal DCR value.

Additionally, in order to improve the accuracy of the current measurement, which can be adversely affected by the temperature coefficient of the inductor’s DCR, the ZSPM1035A features temperature compensation via external temperature sensing. The temperature of the inductors is measured with an external temperature-sensing element placed close to the inductor. This information is used to adapt the gain of the current sense path to compensate for the increase in actual DCR.

3.3.7. Temperature Measurement

The ZSPM1035A features two independent temperature measurement units. The internal temperature sensing measures the temperatures inside the ZSPM1035A. The external temperature sensor is placed on the Murata Power Block. The ZSPM1035A drives 60µA into the external temperature-sensing element and measures the voltage on the TEMP pin. The Pink Power Designer™ GUI must be used to select the offset for configuration of the external temperature measurement. A temperature-offset calibration is highly recommended.

3.4. Fault Monitoring and Response Generation

The ZSPM1035A monitors various signals during operation. Depending on the selected configuration, it can respond to events generated by these signals. A wide range of options is configurable via the Pink Power Designer™. Typical monitoring within the ZSPM1035A is a three-step process. First, an event is detected via a configurable set of thresholds. This event is then digitally filtered before the ZSPM1035A reacts with a defined response depending on the fault condition. For most monitored signals, a warning and a fault threshold can be configured. A warning typically sets a status flag (see section 4.7.6) but does not trigger a response; whereas a fault also generates a response.

The warning and fault events can be enabled for each parameter that the ZSPM1035A monitors (see Table 3.1). The SMBALERT signal is asserted by the ZSPM1035A for any warning or fault that has been enabled. An overview of the faults that the ZSPM1035A can detect and the response to each fault is given in Table 3.1.

Table 3.1 Fault Configuration Overview

| Fault | Response Type |
|---------------------------|---------------|
| Output Over-Voltage | Low impedance |
| Output Under-Voltage | Low impedance |
| Input Over-Voltage | Off |
| Input Under-Voltage | Off |
| Over-Current | Low impedance |
| External Over-Temperature | Off |
| Internal Over-Temperature | Off |

The ZSPM1035A supports different response types depending on the fault detected. An “Off” response ramps the output voltage down using the falling-edge sequencer settings. The final state of the output signals depends on the value selected for V_{OFF_nom} . The “low-impedance” response clamps the PWM output to PGND.

The controller fault handling will infinitely try to restart the converter on a fault condition. In analog controllers, this infinite re-try feature is also known as “hiccup mode.”

3.4.1. Output Over/Under-Voltage

To prevent damage to the load, the ZSPM1035A utilizes an output over-voltage protection circuit. The voltage at VFBP is continuously compared with a configurable fault threshold using a high-speed analog comparator. The fault threshold can be configured using the Pink Power Designer™ GUI. If the voltage exceeds the configured threshold, the fault response is generated and the PWM output is set to low impedance (clamped to PGND). The voltage fault level is generated by a 6-bit DAC with a reference voltage of 1.60V resulting in 25mV resolution.

The output voltage is also sampled using the HKADC and continuously compared to a configurable output over-voltage warning threshold. The warning threshold can be configured using the Pink Power Designer™ GUI. If the output voltage exceeds this threshold, a warning is generated.

The ZSPM1035A also monitors the output voltage with two lower thresholds. If the output voltage is below the under-voltage warning level and above the under-voltage fault level, an output voltage under-voltage warning is triggered. If the output voltage falls below the fault level, a fault event is generated and the output is set to low impedance.

3.4.2. Output Current Protection and Limiting

The ZSPM1035A continuously monitors the average inductor current and utilizes this information to protect the power supply against excessive output current. The output over-current warning and fault threshold levels can be configured using the Pink Power Designer™ GUI. If the fault level is exceeded, the PWM output is set to low impedance.

3.4.3. Over-Temperature Protection

The ZSPM1035A monitors internal and external temperature. For each, a warning and a fault level can be configured and an appropriate response can be enabled.

3.5. Configuration

The ZSPM1035A incorporates two different sets of configuration parameters (see section 4.4). The first set of configuration parameters can be configured during design time and cannot be changed during run-time. The second set of configuration parameters can be configured during design time, but can also be reconfigured during run-time using the appropriate PMBus™ command. Note that the second set of reconfigured values is not stored in the OTP memory, so they are lost during power cycling the device.

In order to evaluate the device and its configuration on the bench, a special engineering mode is supported by the device and Pink Power Designer™. In this engineering mode, the device can be reconfigured multiple times without writing the configuration into the OTP. During this mode, the device starts up after power-on reset in an unconfigured state. The Pink Power Designer™ then provides the configuration to the ZSPM1035A, enabling full operation without actually configuring the OTP. The engineer can use this mode to evaluate the configuration on the bench. However, the configuration will be lost upon power-on-reset.

After the design engineer has determined the final configuration options, an OTP image can be created that is then written into the ZSPM1035A. This can be either on the bench using the Pink Power Designer™ or in end-of-line testing during mass production.

4 PMBus™ Functionality

4.1. Introduction

The ZSPM1035A supports the PMBus™ protocol to enable configuration, monitoring, and fault management during run-time.

The PMBus™ host controller is connected to the ZSPM1035A via the PMBus™ pins (SDA and SCL). A dedicated SMBALERT pin is provided to notify the host that new status information is present.

The ZSPM1035A supports packet error correction (PEC) according to the PMBus™ specification.

4.2. Timing and Bus Specification

Timing for the PMBus™ signals is given in Figure 4.1. The PMBus™ signal SMBCLK is the shift clock input on the SCL pin on the ZSPM1035A (slave only) and the SMBDAT signal is the shift data input/output on the SDA pin.

Figure 4.1 PMBus™ Timing Diagram

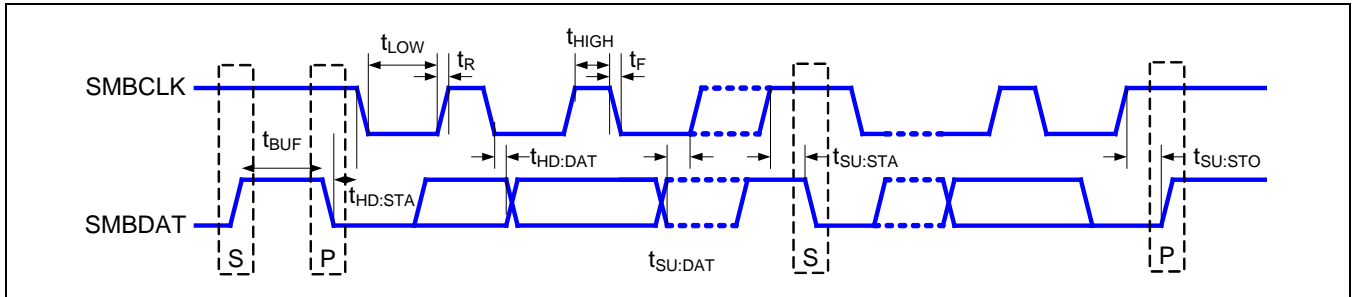


Table 4.1 PMBus™ Timing Specification

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|----------------|------------|-----|-----|-----|---------|
| SMBus operation frequency | f_{SMB} | | 10 | 400 | 500 | kHz |
| Bus free time between start and stop | t_{BUF} | | 1.3 | | | μs |
| Hold time after start condition | $t_{HD:STA}$ | | 0.6 | | | μs |
| Repeat start condition setup time | $t_{SU:STA}$ | | 0.6 | | | μs |
| Stop condition setup time | $t_{SU:STO}$ | | 0.6 | | | μs |
| Data hold time | $t_{HD:DAT}$ | | 300 | | | ns |
| Data setup time | $t_{SU:DAT}$ | | 100 | | | ns |
| Clock low time-out | $t_{TIMEOUT}$ | | | 25 | 35 | μs |
| Clock low period | t_{LOW} | | 1.3 | | | μs |
| Clock high period | t_{HIGH} | | 0.6 | | | μs |
| Cumulative clock low extend time | $t_{LOW:SEXT}$ | | | | 25 | ms |
| Clock or data fall time | t_F | | | | 300 | ns |
| Clock or data rise time | t_R | | | | 300 | ns |

4.3. Address Selection via External Resistors

PMBus™ uses a 7-bit device address to identify different devices connected to the bus. This address can be selected via external resistors connected to the ADDR_x pins.

The resistor values are sensed using the internal ADC during the initialization phase and the appropriate PMBus™ address is selected. Note that the respective circuitry is only active during the initialization phase; hence no DC voltage can be measured at the pins. The supported PMBus™ addresses and the values of the respective required resistors are listed in Table 4.2.

Table 4.2 Supported Resistor Values for PMBus™ Address Selection

| Address (Hex) | ADDR1 Ω | ADDR0 Ω | Address (Hex) | ADDR1 Ω | ADDR0 Ω | Address (Hex) | ADDR1 Ω | ADDR0 Ω | Address (Hex) | ADDR1 Ω | ADDR0 Ω |
|---------------|---------|---------|---------------|---------|---------|---------------|---------|---------|---------------|---------|---------|
| 64 | 0 | 0 | 32 | 1.2 k | 0 | 64 | 2.7 k | 0 | 96 | 4.7 k | 0 |
| 1* | 0 | 680 | 33 | 1.2 k | 680 | 65 | 2.7 k | 680 | 97* | 4.7 k | 680 |
| 2* | 0 | 1.2k | 34 | 1.2 k | 1.2 k | 66 | 2.7 k | 1.2 k | 98 | 4.7 k | 1.2 k |
| 3* | 0 | 1.8k | 35 | 1.2 k | 1.8 k | 67 | 2.7 k | 1.8 k | 99 | 4.7 k | 1.8 k |
| 4* | 0 | 2.7k | 36 | 1.2 k | 2.7 k | 68 | 2.7 k | 2.7 k | 100 | 4.7 k | 2.7 k |
| 5* | 0 | 3.9k | 37 | 1.2 k | 3.9 k | 69 | 2.7 k | 3.9 k | 101 | 4.7 k | 3.9 k |
| 6* | 0 | 4.7k | 38 | 1.2 k | 4.7 k | 70 | 2.7 k | 4.7 k | 102 | 4.7 k | 4.7 k |
| 7* | 0 | 5.6k | 39 | 1.2 k | 5.6 k | 71 | 2.7 k | 5.6 k | 103 | 4.7 k | 5.6 k |
| 8* | 0 | 6.8k | 40* | 1.2 k | 6.8 k | 72 | 2.7 k | 6.8 k | 104 | 4.7 k | 6.8 k |
| 9 | 0 | 8.2k | 41 | 1.2 k | 8.2 k | 73 | 2.7 k | 8.2 k | 105 | 4.7 k | 8.2 k |
| 10 | 0 | 10k | 42 | 1.2 k | 10 k | 74 | 2.7 k | 10 k | 106 | 4.7 k | 10 k |
| 11 | 0 | 12k | 43 | 1.2 k | 12 k | 75 | 2.7 k | 12 k | 107 | 4.7 k | 12 k |
| 12* | 0 | 15k | 44 | 1.2 k | 15 k | 76 | 2.7 k | 15 k | 108 | 4.7 k | 15 k |
| 13 | 0 | 18k | 45 | 1.2 k | 18 k | 77 | 2.7 k | 18 k | 109 | 4.7 k | 18 k |
| 14 | 0 | 22k | 46 | 1.2 k | 22 k | 78 | 2.7 k | 22 k | 110 | 4.7 k | 22 k |
| 15 | 0 | 27k | 47 | 1.2 k | 27 k | 79 | 2.7 k | 27 k | 111 | 4.7 k | 27 k |
| 16 | 680 | 0 | 48 | 1.8 k | 0 | 80 | 3.9 k | 0 | 112 | 5.6 k | 0 |
| 17 | 680 | 680 | 49 | 1.8 k | 680 | 81 | 3.9 k | 680 | 113 | 5.6 k | 680 |
| 18 | 680 | 1.2k | 50 | 1.8 k | 1.2 k | 82 | 3.9 k | 1.2 k | 114 | 5.6 k | 1.2 k |
| 19 | 680 | 1.8k | 51 | 1.8 k | 1.8 k | 83 | 3.9 k | 1.8 k | 115 | 5.6 k | 1.8 k |
| 20 | 680 | 2.7k | 52 | 1.8 k | 2.7 k | 84 | 3.9 k | 2.7 k | 116 | 5.6 k | 2.7 k |
| 21 | 680 | 3.9k | 53 | 1.8 k | 3.9 k | 85 | 3.9 k | 3.9 k | 117 | 5.6 k | 3.9 k |
| 22 | 680 | 4.7k | 54 | 1.8 k | 4.7 k | 86 | 3.9 k | 4.7 k | 118 | 5.6 k | 4.7 k |
| 23 | 680 | 5.6k | 55* | 1.8 k | 5.6 k | 87 | 3.9 k | 5.6 k | 119 | 5.6 k | 5.6 k |
| 24 | 680 | 6.8k | 56 | 1.8 k | 6.8 k | 88 | 3.9 k | 6.8 k | 120* | 5.6 k | 6.8 k |
| 25 | 680 | 8.2k | 57 | 1.8 k | 8.2 k | 89 | 3.9 k | 8.2 k | 121* | 5.6 k | 8.2 k |
| 26 | 680 | 10k | 58 | 1.8 k | 10 k | 90 | 3.9 k | 10 k | 122* | 5.6 k | 10 k |
| 27 | 680 | 12k | 59 | 1.8 k | 12 k | 91 | 3.9 k | 12 k | 123* | 5.6 k | 12 k |
| 28 | 680 | 15k | 60 | 1.8 k | 15 k | 92 | 3.9 k | 15 k | 124* | 5.6 k | 15 k |
| 29 | 680 | 18k | 61 | 1.8 k | 18 k | 93 | 3.9 k | 18 k | 125* | 5.6 k | 18 k |
| 30 | 680 | 22k | 62 | 1.8 k | 22 k | 94 | 3.9 k | 22 k | 126* | 5.6 k | 22 k |
| 31 | 680 | 27k | 63 | 1.8 k | 27 k | 95 | 3.9 k | 27 k | 127* | 5.6 k | 27 k |

Note: The addresses marked with an asterisk (*) are reserved by the SMBus specification.

If only four devices are used in a system, their respective addresses can alternatively be configured without resistors by connecting the pins to GND or the AVDD18 pin. The PMBus™ addresses selectable in this fashion are listed in Table 4.3.

Table 4.3 PMBus™ Address Selection without Resistors

| Address | ADDR1 | ADDR0 |
|---------|--------|--------|
| 15 | GND | AVDD18 |
| 48 | AVDD18 | GND |
| 63 | AVDD18 | AVDD18 |
| 64 | GND | GND |

4.4. Configuration Registers

Two different sets of configuration parameters are supported by the ZSPM1035A. The first set of parameters can only be configured during the configuration phase of the ZSPM1035A. These values are written into the OTP memory and cannot be changed using PMBus™ commands during run-time. A second set of parameters can also be configured during run-time using the appropriate PMBus™ commands. The two groups are classified in the PMBus™ configuration table (Table 4.4).

Table 4.4 List of Supported PMBus™ Configuration Registers

Note: See important notes at the end of the table.

| PMBus™ Parameter | Description | Data Format | Classification |
|-------------------------------|---|-----------------------|----------------|
| Output Voltage | | | |
| ON_OFF_CONFIG | On/off configuration | N/A | PMBus™ |
| VOUT_MODE | Exponent of the VOUT_COMMAND value | N/A | Read only |
| VOUT_COMMAND | Set output voltage | LINEAR ⁽¹⁾ | PMBus™ |
| VOUT_OV_FAULT_LIMIT | Over-voltage fault limit | N/A | OTP |
| VOUT_OV_WARN_LIMIT | Over-voltage warning level | N/A | OTP |
| VOUT_UV_WARN_LIMIT | Under-voltage warning level | N/A | OTP |
| VOUT_UV_FAULT_LIMIT | Under-voltage fault level | N/A | OTP |
| Output Current | | | |
| IOUT_OC_FAULT_LIMIT | Over-current fault limit | N/A | OTP |
| IOUT_OC_WARN_LIMIT | Over-current warning level | N/A | OTP |
| Temperature – External | | | |
| OT_FAULT_LIMIT | External over-temperature fault level | N/A | OTP |
| OT_WARN_LIMIT | External over-temperature warning level | N/A | OTP |
| Temperature – Internal | | | |
| IOT_FAULT_LIMIT | Internal over-temperature fault level | N/A | OTP |
| IOT_WARN_LIMIT | Internal over-temperature warning level | N/A | OTP |
| Input Voltage | | | |
| VIN_OV_FAULT_LIMIT | Over-voltage fault limit | N/A | OTP |

| PMBus™ Parameter | Description | Data Format | Classification |
|---|-------------------------------|-------------|----------------|
| VIN_OV_WARN_LIMIT | Over-voltage warning level | N/A | OTP |
| VIN_UV_WARN_LIMIT | Under-voltage warning level | N/A | OTP |
| VIN_UV_FAULT_LIMIT | Under-voltage fault level | N/A | OTP |
| Start-up Behavior / Power Sequencing | | | |
| POWER_GOOD_ON | Power good on threshold | N/A | OTP |
| POWER_GOOD_OFF | Power good off threshold | N/A | OTP |
| Output Voltage Sequencing | | | |
| TON_DELAY | Turn-on delay | N/A | OTP |
| TON_RISE | Turn-on rise time | N/A | OTP |
| TON_FAULT_MAX | Turn-on maximum fault time | N/A | OTP |
| TOFF_DELAY | Turn-off delay | N/A | OTP |
| TOFF_FALL | Turn-off fall time | N/A | OTP |
| TOFF_WARN_MAX | Turn-off maximum warning time | N/A | OTP |
| VOFF_NOM | Soft-stop off value | N/A | OTP |
| Notes: | | | |
| 1. VOUT_MODE is read-only for this device. | | | |

The ZSPM1035A supports the LINEAR data format according to the PMBus™ specification. Note that in accordance with the PMBus™ specification, all commands related to the output voltage are subject to the VOUT_MODE settings. Note that VOUT_MODE is read-only for the ZSPM1035A.

4.5. Monitoring

The ZSPM1035A has a dedicated set of PMBus™ registers to enable advanced power management using extensive monitoring features. Different warning and error flags can be read by the PMBus™ master to ensure proper operation of the power converter or monitor the converters over the product lifetime.

Table 4.5 List of Supported PMBus™ Status Registers

| PMBus™ Command | Description | Data Format |
|--------------------|---------------------------------|-------------|
| CLEAR_FAULTS | Clear status information | |
| STATUS_BYTE | Unit status byte | |
| STATUS_WORD | Unit status word | |
| STATUS_VOUT | Output voltage status | |
| STATUS_IOUT | Output current status | |
| STATUS_INPUT | Input status | |
| STATUS_TEMPERATURE | Temperature status | |
| STATUS_CML | Communication and memory status | |
| READ_VIN | Input voltage read back | LINEAR |
| READ_VOUT | Output voltage read back | LINEAR |
| READ_IOUT | Output current read back | LINEAR |
| READ_TEMPERATURE_1 | External temperature read back | LINEAR |
| READ_TEMPERATURE_2 | Internal temperature read back | LINEAR |

4.6. Additional Registers

Table 4.6 Additional Supported PMBus™ Registers

| PMBus™ Command | Description | Data Length (Byte) | Values |
|----------------|-------------------------------|--------------------|--|
| PMBUS_REVISION | PMBus™ revision | 1 | 11 _{HEX} |
| MFR_ID | Manufacturer ID | 4 | “ZMDI” (5A _{HEX} , 4D _{HEX} , 44 _{HEX} , 49 _{HEX}) |
| MFR_MODEL | Manufacturer model identifier | 4 | “1035” (31 _{HEX} , 30 _{HEX} , 33 _{HEX} , 35 _{HEX}) |
| MFR_REVISION | Manufacturer product revision | 4 | |
| MFR_SERIAL | Serial number | 12 | |

4.7. Detailed Description of the Supported PMBus™ Commands

4.7.1. OPERATION

The OPERATION command is used to turn the unit on and off in conjunction with the input from the CONTROL pin. The unit stays in the commanded operating mode until a subsequent OPERATION command or change in the state of the CONTROL pin instructs the device to change to another mode. The supported operation modes are listed in Table 4.7.

Table 4.7 Supported PMBus™ Operation Modes

| OPERATION (read/write) | | | | | |
|------------------------|-----------|-----------|-----------|----------------------------|--------------|
| Bits[7:6] | Bits[5:4] | Bits[3:2] | Bits[1:0] | Unit On or Off | Margin State |
| 01 | XX | XX | XX | Soft Off (With Sequencing) | N/A |
| 10 | 00 | XX | XX | On | Off |

4.7.2. ON_OFF_CONFIG

The ON_OFF_CONFIG command is used to configure the combination of the CONTROL pin and the PMBus™ OPERATION command that turns the unit on or off. The supported configuration options are listed in Table 4.8.

Table 4.8 Supported PMBus™ ON_OFF_CONFIG Options

| ON_OFF_CONFIG (read/write) | | |
|----------------------------|------------------|--|
| Bits | Name | Description |
| [0] | CONTROL OFF | Value ignored. Device always uses the programmed turn off delay and fall time. |
| [1] | CONTROL Polarity | 0: Active low (pull pin low to start the unit). 1: Active high (pull pin high to start the unit). |
| [2] | CONTROL Enable | 0: Unit ignores the CONTROL pin. 1: Unit requires the CONTROL pin to be asserted to start the unit.* |
| [3] | OPERATION Enable | 0: Unit ignores the on/off settings in the OPERATION command. 1: Unit requires the on/off settings in the OPERATION command to start the unit*. |

* Depending on the configuration, both conditions must be in the on state in order to turn on the unit.

4.7.3. CLEAR_FAULTS

The CLEAR_FAULTS command is used to clear any fault bits that have been set in the status registers. Additionally, the SMBALERT signal is cleared if it was previously asserted. Note that the device resumes operation with the currently configured state after a CLEAR_FAULTS command has been issued. If a fault/warning is still present, the respective bit is set immediately again.

4.7.4. VOUT_MODE

The VOUT_MODE command is used to retrieve information about the data format for all output voltage related commands. Note that this is a read-only value.

| VOUT_MODE (read only) | | |
|-----------------------|-----------|--------------------------------|
| Bits | Name | Description |
| [4:0] | PARAMETER | 2's complement of the exponent |
| [7:5] | MODE | 000: Linear data format |

4.7.5. VOUT_COMMAND

The VOUT_COMMAND is used to set the output voltage during run-time.

Note that the maximum output voltage is 3.6V.

| VOUT_COMMAND (read/write) | | |
|---------------------------|----------|---|
| Bits | Name | Description |
| [15:0] | MANTISSA | Unsigned mantissa of output voltage in volts. Exponent can be retrieved via VOUT_MODE command. |

4.7.6. STATUS_BYTE

The STATUS_BYTE command returns a summary of the most critical faults in one byte.

| STATUS_BYTE (read only) | | |
|-------------------------|-------------------|--|
| Bits | Name | Description |
| [0] | NONE OF THE ABOVE | A fault not listed in bits [7:1] has occurred. |
| [1] | CML | A communication fault as occurred. |
| [2] | TEMPERATURE | A temperature fault or warning has occurred. |
| [3] | VIN_UV | An input under-voltage fault has occurred. |
| [4] | IOUT_OC | An output over-current fault has occurred. |
| [5] | VOUT_OV | An output over-voltage fault has occurred. |
| [6] | OFF | This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. |
| [7] | BUSY | Not supported. |

4.7.7. STATUS_WORD

The STATUS_WORD command returns a summary of the device status information in two data bytes.

| STATUS_WORD (read only) | | |
|-------------------------|-------------|--|
| Bits | Name | Description |
| [7:0] | STATUS_BYTE | See status byte (section 4.7.6). |
| [8] | UNKNOWN | Not supported |
| [9] | OTHER | Not supported |
| [10] | FANS | No supported |
| [11] | POWER_GOOD# | The POWER_GOOD signal, if present, is negated. |
| [12] | MFR | A manufacturer-specific fault or warning has occurred. |
| [13] | INPUT | An input-related warning or fault has occurred. |
| [14] | IOUT/POUT | An output current or output power warning or fault has occurred. |
| [15] | VOUT | An output-voltage-related warning or fault has occurred. |

4.7.8. STATUS_VOUT

| STATUS_VOUT (read only) | | |
|-------------------------|--------------|---|
| Bits | Name | Description |
| [0] | | Not supported. |
| [1] | | Not supported. |
| [2] | | Not supported. |
| [3] | | Not supported. |
| [4] | VOUT_UV_FLT | An output voltage under-voltage fault has occurred. |
| [5] | VOUT_UV_WARN | An output voltage under-voltage warning has occurred. |
| [6] | VOUT_OV_WARN | An output voltage over-voltage warning has occurred. |
| [7] | VOUT_OV_FLT | An output voltage over-voltage fault has occurred. |

4.7.9. STATUS_IOUT

| STATUS_IOUT (read only) | | |
|-------------------------|--------------|---------------------------------------|
| Bits | Name | Description |
| [0] | | Not supported. |
| [1] | | Not supported. |
| [2] | | Not supported. |
| [3] | | Not supported. |
| [4] | | Not supported. |
| [5] | IOUT_OC_WARN | An over-current warning has occurred. |
| [6] | | Not supported. |
| [7] | IOUT_OC_FLT | An over-current fault has occurred. |

4.7.10. STATUS_INPUT

| STATUS_INPUT (read only) | | |
|--------------------------|-------------|--|
| Bits | Name | Description |
| [0] | | Not supported. |
| [1] | | Not supported. |
| [2] | | Not supported. |
| [3] | | Not supported. |
| [4] | VIN_UV_FLT | An input voltage under-voltage fault has occurred. |
| [5] | VIN_UV_WARN | An input voltage under-voltage warning has occurred. |
| [6] | VIN_OV_WARN | An input voltage over-voltage warning has occurred. |
| [7] | VIN_OV_FLT | An input voltage over-voltage fault has occurred. |

4.7.11. STATUS_TEMPERATURE

| STATUS_TEMPERATURE (read only) | | |
|--------------------------------|--------------|--|
| Bits | Name | Description |
| [0] | | Not supported. |
| [1] | | Not supported. |
| [2] | | Not supported. |
| [3] | | Not supported. |
| [4] | | Not supported. |
| [5] | | Not supported. |
| [6] | TEMP_OV_WARN | An (external) over-temperature warning has occurred. |
| [7] | TEMP_OV_FLT | An (external) over-temperature fault has occurred. |

4.7.12. STATUS_CML

| STATUS_CML (read only) | | |
|------------------------|-----------|---|
| Bits | Name | Description |
| [0] | | Not supported. |
| [1] | SMBUS_FLT | SMBus™ timeout or a format error has occurred. |
| [2] | | Not supported. |
| [3] | | Not supported. |
| [4] | | Not supported. |
| [5] | PEC_FLT | A packet error check fault has occurred. |
| [6] | | Not supported. |
| [7] | CMD_FLT | An invalid or an unsupported command has been received. |

4.7.13. STATUS_MFR_SPECIFIC

| STATUS_MFR_SPECIFIC (read only) | | |
|---------------------------------|---------------|--|
| Bits | Name | Description |
| [0] | | Not supported. |
| [1] | | Not supported. |
| [2] | | Not supported. |
| [3] | | Not supported. |
| [4] | | Not supported. |
| [5] | | Not supported. |
| [6] | ITEMP_OV_WARN | An (internal) over-temperature warning has occurred. |
| [7] | ITEMP_OV_FLT | An (internal) over-temperature fault has occurred. |

4.7.14. READ_VIN

| READ_VIN (read only) | | |
|----------------------|------|--|
| Bits | Name | Description |
| [15:0] | VIN | Input voltage in V (linear data format). |

4.7.15. READ_VOUT

| READ_VOUT (read only) | | |
|-----------------------|------|---|
| Bits | Name | Description |
| [15:0] | VOUT | Output voltage in V (linear data format). Note that this command is mantissa only. |

4.7.16. READ_IOUT

| READ_IOUT (read only) | | |
|-----------------------|------|---|
| Bits | Name | Description |
| [15:0] | IOUT | Output current in A (linear data format). |

4.7.17. READ_TEMPERATURE1

| READ_TEMPERATURE1 (read only) | | |
|-------------------------------|-------|--|
| Bits | Name | Description |
| [15:0] | TEMP1 | External temperature in °C (linear data format). |

4.7.18. READ_TEMPERATURE2

| READ_TEMPERATURE2 (read only) | | |
|-------------------------------|-------|--|
| Bits | Name | Description |
| [15:0] | TEMP2 | Internal temperature in °C (linear data format). |

5 Application Information

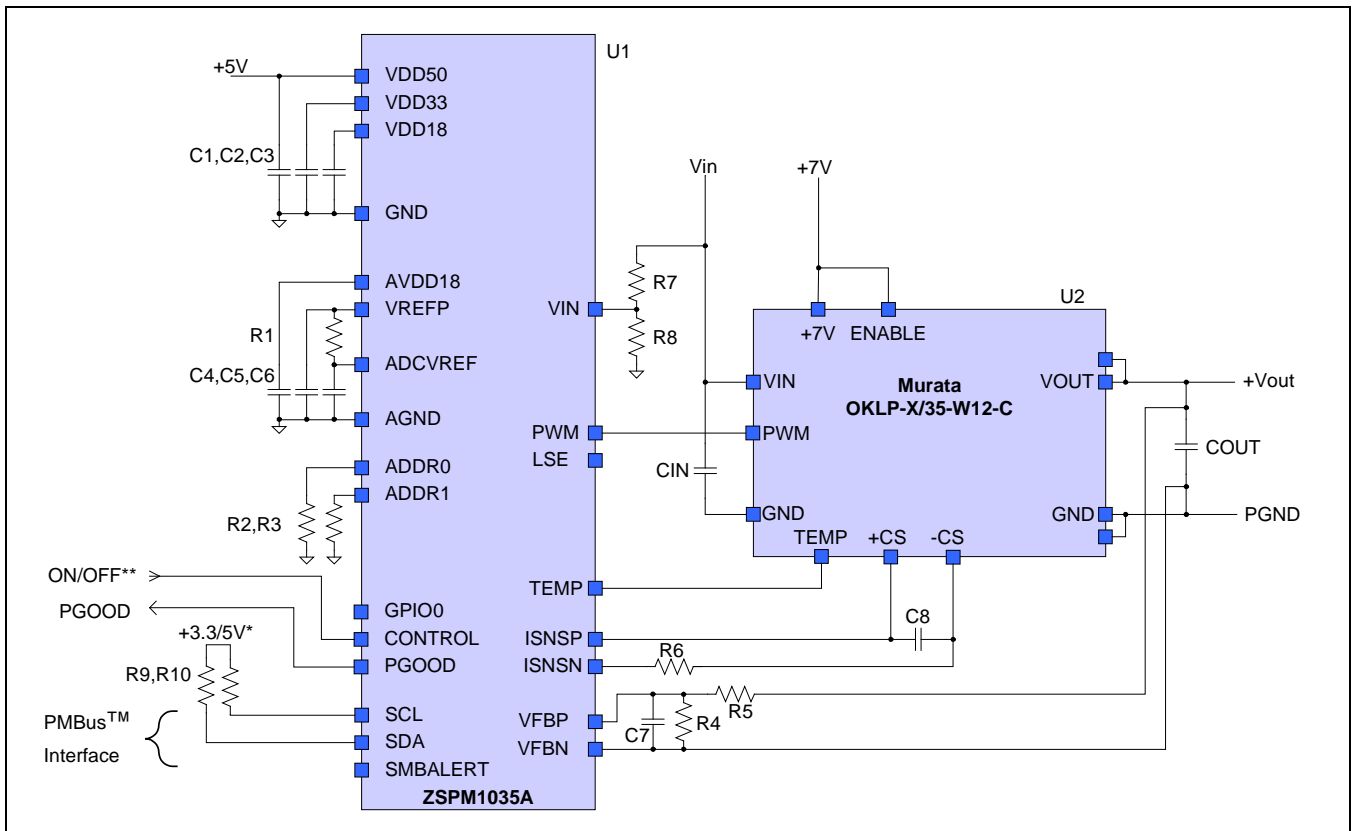
The ZSPM1035A has been designed and pre-configured to operate with the Murata OKLP-X/35-W12-C Power Block, which is a complete point-of-load solution for 35A output currents. This section includes information about the typical application circuit and recommended component values. IDT provides ZSPM1035A configuration data that is downloadable from IDT website as part of the Pink Power Designer™ GUI. While the solution is pre-configured, the design engineer has the flexibility to configure the output voltage and select one of the four pre-defined and common output capacitor ranges.

Included in the Pink Power Designer™ software is a wizard dialog for guiding the user through the design process step-by-step, which makes it a ready-made, easy, and tested solution.

5.1. Typical Application Circuit

A schematic for the typical application circuit is shown in Figure 5.1. A list of recommended component values for the passive components can be found in Table 5.1.

Figure 5.1 Application Circuit with a 5V Supply Voltage



Notes:

- * PMBus™ SCL and SDA pull-up resistors R9/R10 can be tied to 3.3V or 5V depending on the PMBus™ master controller.
- ** The ON/OFF input can be active high or active low depending on the configuration of the CONTROL pin on the ZSPM1035A.

Table 5.1 *Passive Component Values for the Application Circuit*

| Reference Designator | Component Value | Description |
|----------------------|------------------|--|
| C1 | 1.0 μ F | Ceramic capacitor. |
| C2 | 4.7 μ F | Ceramic capacitor. Recommended 4.7 μ F, Minimum 1.0 μ F. |
| C3 | 4.7 μ F | Ceramic capacitor. Recommended 4.7 μ F, Minimum 1.0 μ F. |
| C4 | 4.7 μ F | Ceramic capacitor. Recommended 4.7 μ F, Minimum 1.0 μ F. |
| C5 | 4.7 μ F | Ceramic capacitor. Recommended 4.7 μ F, Minimum 1.0 μ F. |
| C6 | 100nF | |
| C7 | 22pF | Output voltage sense filtering capacitor. Recommended 22pF, maximum 1nF. |
| C8 | 220nF* | DCR current-sense filter capacitor. |
| CIN | | Input filter capacitors. Can be a combination of ceramic and electrolytic capacitors. |
| COUT | | Output filter capacitors. See section 5.1.2 for more information on the output capacitor selection. |
| R1 | 51 Ω * | |
| R2, R3 | | Select PMBus™ address resistor value from Table 4.2. |
| R4 | 1.0k Ω * | Output voltage divider bottom resistor. Connect between the VFBP and VFBN pins. Populate R4 only if the output voltage range is from 1.20V to 3.60V. Do not populate R4 if the output voltage is below 1.20V. See section 5.1.1. |
| R5 | 1.74k Ω * | Output voltage divider top resistor. Connect between the output terminal and the VFBP pin. |
| R6 | 2.15k Ω * | DCR current sense filter resistor. |
| R7 | 9.1k Ω * | Input voltage divider top resistor. Connect between the main power input and the VIN pin of the ZSPM1035A. |
| R8 | 1.0k Ω * | Input voltage divider bottom resistor. Connect between the VIN and AGND pins of the ZSPM1035A. |
| R9, R10 | 15k Ω * | PMBus™ SCL and SDA line pull-up resistors. The pull-up resistors can be tied to 3.3V or 5V depending on the supply voltage of the PMBus™ master. |

* Values marked with an asterisk are fixed component values that must not be changed.

5.1.1. Output Voltage Selection

The ZSPM1035A can be configured to operate within two output voltage ranges (see Table 5.2). If the required output voltage is within range #1 resistor R4 should not be placed on the application board. For output voltages within range #2, resistor R4 should be placed on the application board.

Table 5.2 Output Voltage Ranges

| Output voltage Range | Minimum VOUT | Maximum VOUT |
|----------------------|--------------|--------------|
| #1 | 0.35V | 1.20V |
| #2 | 1.20V | 3.60V |

5.1.2. Output Capacitor Selection

The ZSPM1035A Digital PWM controller can be configured to operate over a wide range of output capacitance. Four ranges of output capacitance have been specified to match typical customer requirements (see Table 5.3).

Typical performance measurements for both load transient performance and open-loop Bode plots can be found in section 5.2. Using less output capacitance than the minimum capacitance given in Table 5.3 is not recommended.

Table 5.3 Recommended Output Capacitor Ranges

| Capacitor Range | Ceramic Capacitor | Bulk Electrolytic Capacitors |
|-----------------|---|---|
| #1 | Minimum 200 μ F Maximum 400 μ F | None |
| #2 | Minimum 400 μ F Maximum 1000 μ F | None |
| #3 | Minimum 100 μ F Maximum 600 μ F | Minimum 2 x 470 μ F, 7m Ω ESR Maximum 5 x 470 μ F, 7m Ω ESR |
| #4 | Minimum 400 μ F Maximum 1000 μ F | Minimum 4 x 470 μ F, 7m Ω ESR Maximum 10 x 470 μ F, 7m Ω ESR |

5.2. Typical Performance Measurements for the ZSPM1035A

IDT has designed eight sets of compensation loop parameters for the ZSPM1035A. The compensation loop parameters have been designed for each of the two output-voltage ranges (see Table 5.2) in combination with one of the four ranges of output capacitors (see Table 5.3). The Pink Power Designer™ GUI wizard can guide the user through a selection process and load the correct set of parameters for the selected output voltage and output capacitor range. Please see the *Pink Power Designer™ GUI User Guide* for more information on the wizard.

Load transient performance measurements and open loop Bode plots for the eight configurations can be found in sections 5.2.1 to 5.2.8. The transient load steps have been generated with a load resistor and a power MOSFET located on the same circuit board as the ZSPM1035A and the Murata OKLP-X/35-W12-C Power Block.

The ZSPM8035 Evaluation Kit can be used to further evaluate the performance of the ZSPM1035A for the four capacitor ranges.

5.2.1. Typical Load Transient Response – Capacitor Range #1 – VOUT Range #1

Test conditions: $V_{IN} = 12.0V$, $V_{OUT} = 1.20V$
 Minimum output capacitance: 2 x 100 μ F/6.3V X5R
 Maximum output capacitance: 3 x 100 μ F/6.3V X5R + 2 x 47 μ F/10V X7R

Figure 5.2 VOUT Range #1 with Capacitor Range #1 – Load Step 5 to 15A, Min. Capacitance

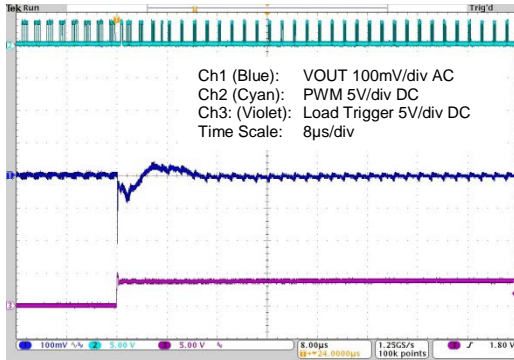


Figure 5.3 VOUT Range #1 with Capacitor Range #1 – Load Step 15 to 5A, Min. Capacitance

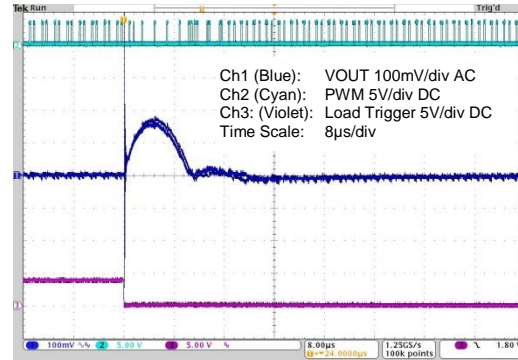


Figure 5.4 VOUT Range #1 with Capacitor Range #1 – Load Step 5 to 15A, Max. Capacitance

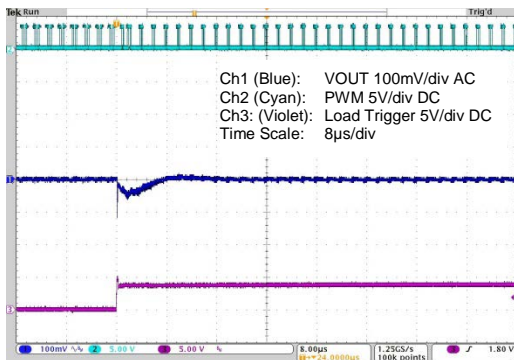


Figure 5.5 VOUT Range #1 with Capacitor Range #1 – Load Step 15 to 5A, Max. Capacitance

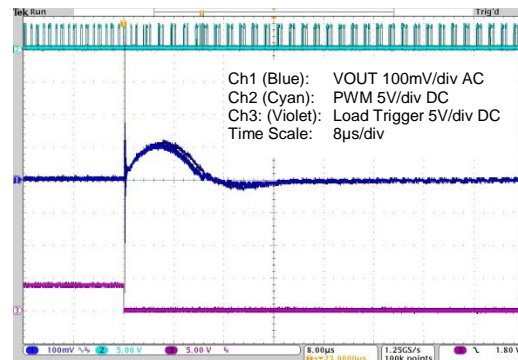
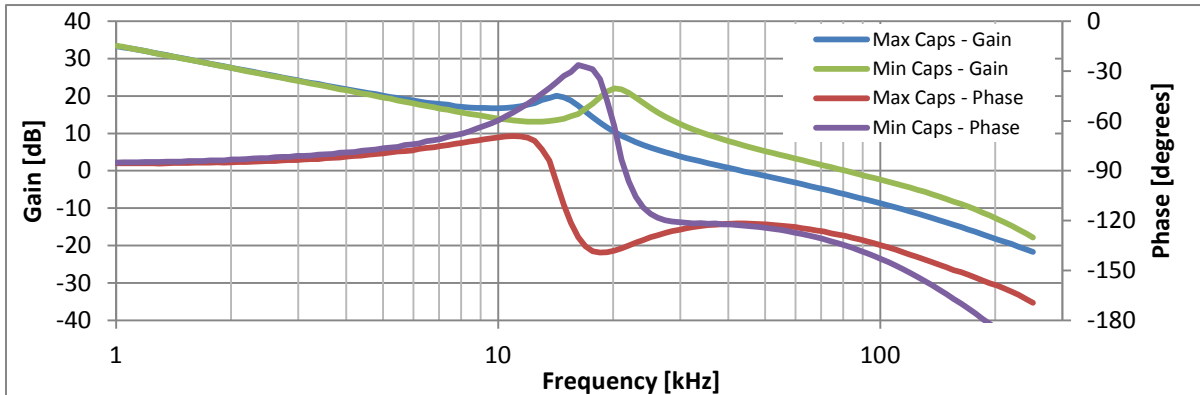


Figure 5.6 Open Loop Bode Plots for VOUT Range #1 with Capacitor Range #1



5.2.2. Typical Load Transient Response – Capacitor Range #2 – VOUT Range #1

Test conditions: $V_{IN} = 12.0V$, $V_{OUT} = 1.20V$

Minimum output capacitance: 3 x 100 μ F/6.3V X5R + 2 x 47 μ F/10V X7R

Maximum output capacitance: 7 x 100 μ F/6.3V X5R + 4 x 47 μ F/10V X7R

Figure 5.7 VOUT Range #1 with Capacitor Range #2 – Load Step 5 to 15A, Min. Capacitance

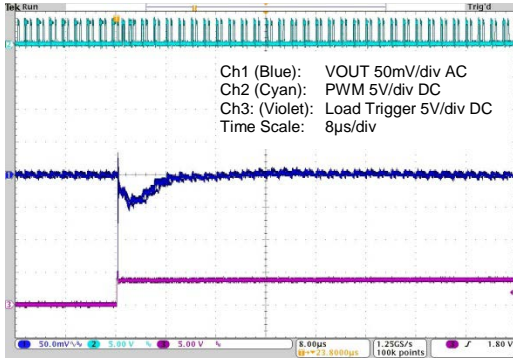


Figure 5.8 VOUT Range #1 with Capacitor Range #2 – Load Step 15 to 5A, Min. Capacitance

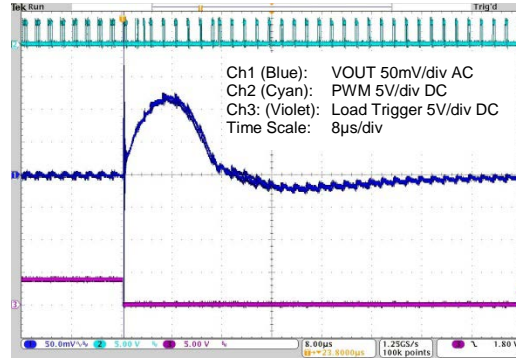


Figure 5.9 VOUT Range #1 with Capacitor Range #2 – Load Step 5 to 15A, Max. Capacitance

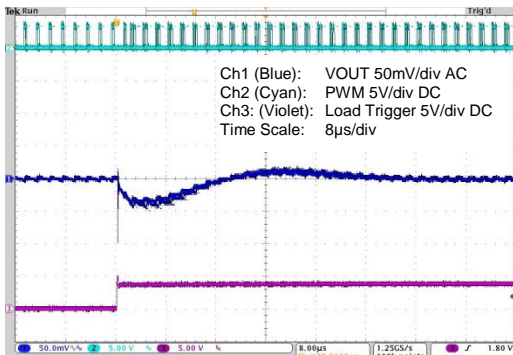


Figure 5.10 VOUT Range #1 with Capacitor Range #2 – Load Step 15 to 5A, Min. Capacitance

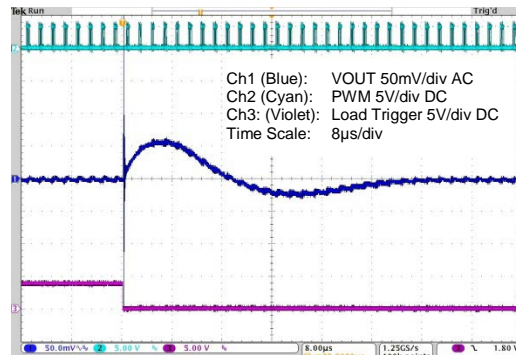
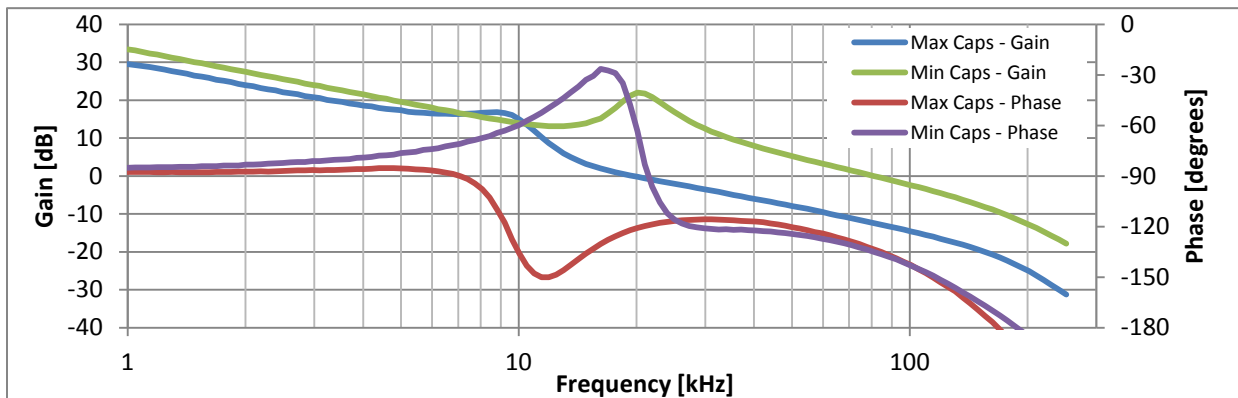


Figure 5.11 Open Loop Bode Plots for VOUT Range #1 with Capacitor Range #2



5.2.3. Typical Load Transient Response – Capacitor Range #3 – VOUT Range #1

Test conditions: $V_{IN} = 12.0V$, $V_{OUT} = 1.20V$

Minimum output capacitance: 1 x 100 μ F/6.3V X5R + 2 x 470 μ F/6.3V/7m Ω Aluminum Electrolytic Capacitor

Maximum output capacitance: 6 x 100 μ F/6.3V X5R + 5 x 470 μ F/6.3V/7m Ω Aluminum Electrolytic Capacitor

Figure 5.12 VOUT Range #1 with Capacitor Range #3 – Load Step 5 to 15A, Min. Capacitance

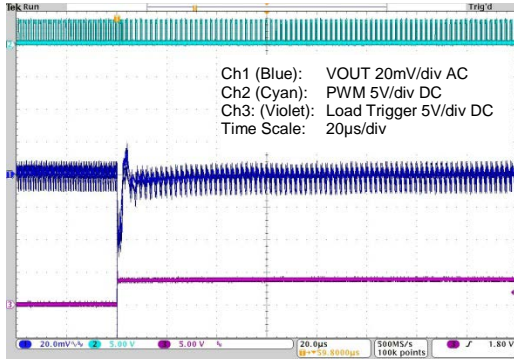


Figure 5.13 VOUT Range #1 with Capacitor Range #3 – Load Step 15 to 5A, Min. Capacitance

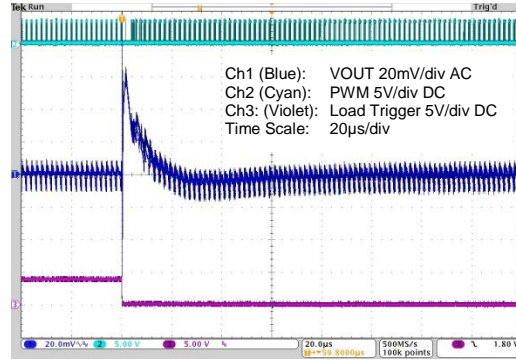


Figure 5.14 VOUT Range #1 with Capacitor Range #3 – Load Step 5 to 15A, Max. Capacitance

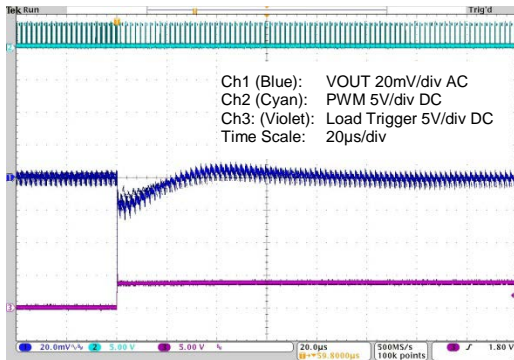


Figure 5.15 VOUT Range #1 with Capacitor Range #3 – Load Step 15 to 5A, Max. Capacitance

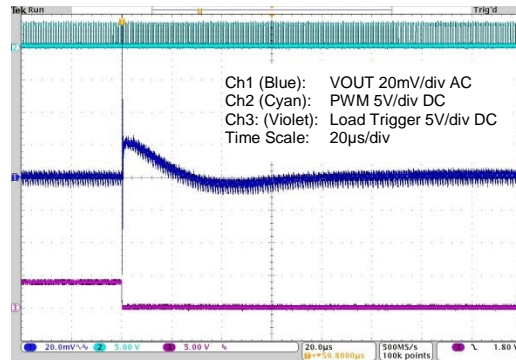
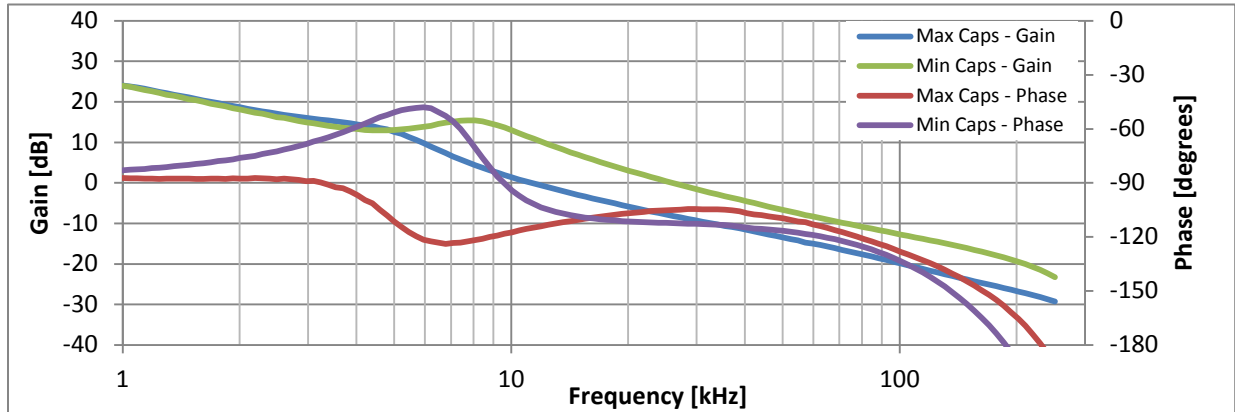


Figure 5.16 Open Loop Bode Plots for VOUT Range #1 with Capacitor Range #3



5.2.4. Typical Load Transient Response – Capacitor Range #4 – VOUT Range #1

Test conditions: $V_{IN} = 12.0V$, $V_{OUT} = 1.20V$

Minimum output capacitance: 3 x 100 μ F/6.3V X5R + 2 x 47 μ F/10V X7R + 4 x 470 μ F/6.3V/7m Ω Aluminum Electrolytic Capacitor

Maximum output capacitance: 7 x 100 μ F/6.3V X5R + 4 x 47 μ F/10V X7R + 10 x 470 μ F/6.3V/7m Ω Aluminum Electrolytic Capacitor

Figure 5.17 VOUT Range #1 with Capacitor Range #4 – Load Step 5 to 15A, Min. Capacitance

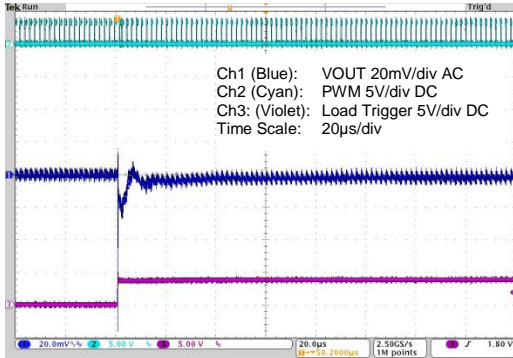


Figure 5.18 VOUT Range #1 with Capacitor Range #4 – Load Step 15 to 5A, Min. Capacitance

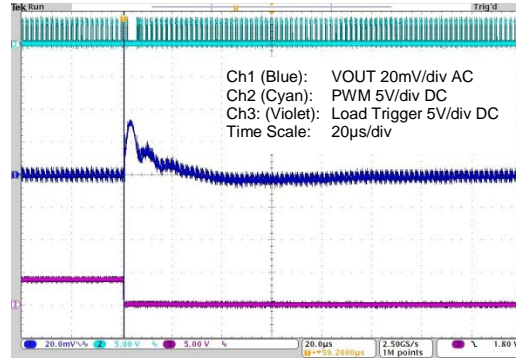


Figure 5.19 VOUT Range #1 with Capacitor Range #4 – Load Step 5 to 15A, Max. Capacitance

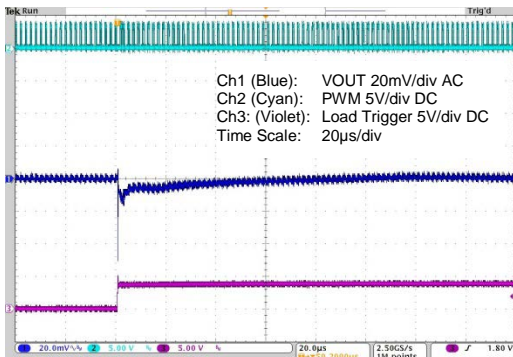


Figure 5.20 VOUT Range #1 with Capacitor Range #4 – Load Step 15 to 5A, Max. Capacitance

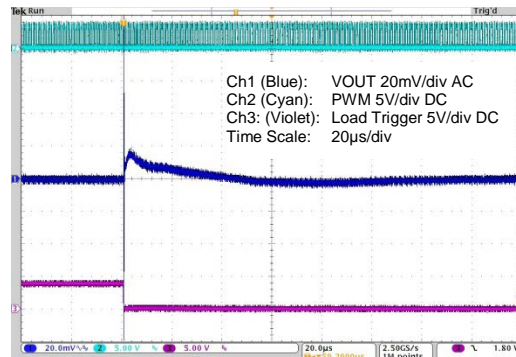
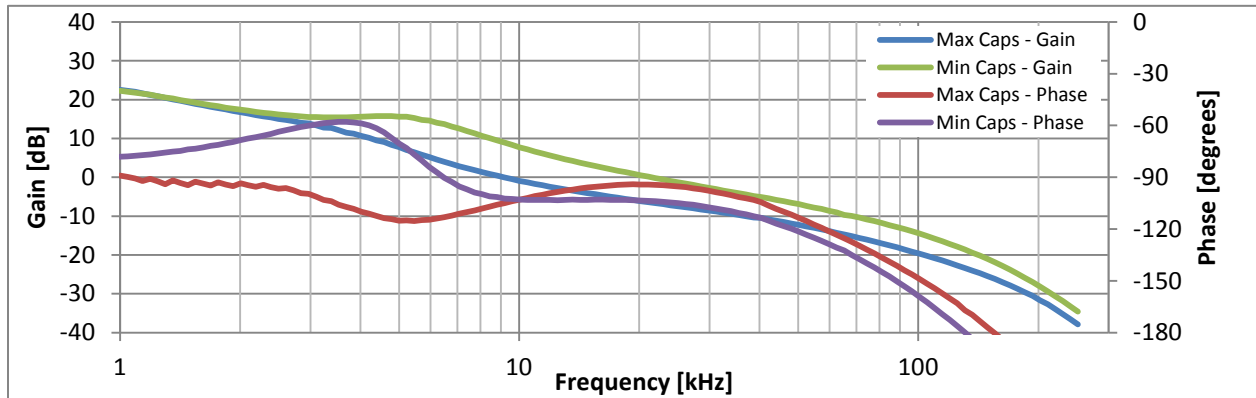


Figure 5.21 Open Loop Bode Plots for VOUT Range #1 with Capacitor Range #4



5.2.5. Typical Load Transient Response – Capacitor Range #1 – VOUT Range #2

Test conditions: $V_{IN} = 12.0V$, $V_{OUT} = 1.80V$

Minimum output capacitance: $2 \times 100\mu F/6.3V \times 5R$

Maximum output capacitance: $3 \times 100\mu F/6.3V \times 5R + 2 \times 47\mu F/10V \times 7R$

Figure 5.22 VOUT Range #2 with Capacitor Range #1 – Load Step 5 to 15A, Min. Capacitance

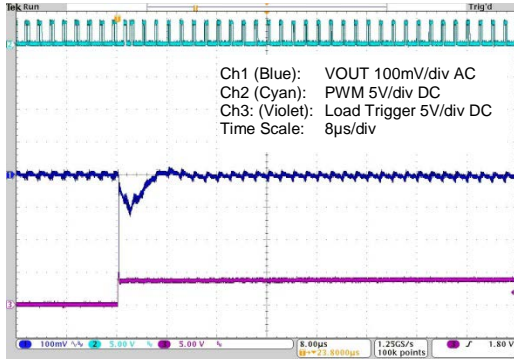


Figure 5.23 VOUT Range #2 with Capacitor Range #1 – Load Step 15 to 5A, Min. Capacitance

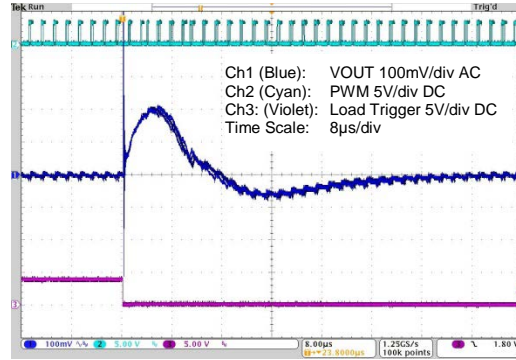


Figure 5.24 VOUT Range #2 with Capacitor Range #1 – Load Step 5 to 15A, Max. Capacitance

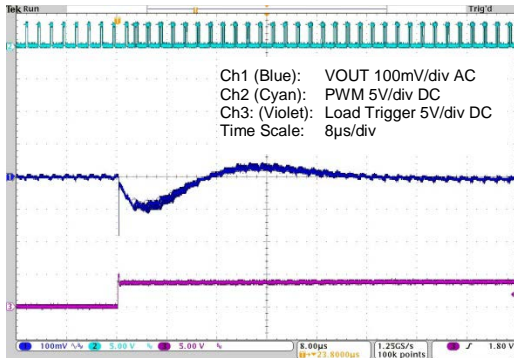


Figure 5.25 VOUT Range #2 with Capacitor Range #1 – Load Step 15 to 5A, Max. Capacitance

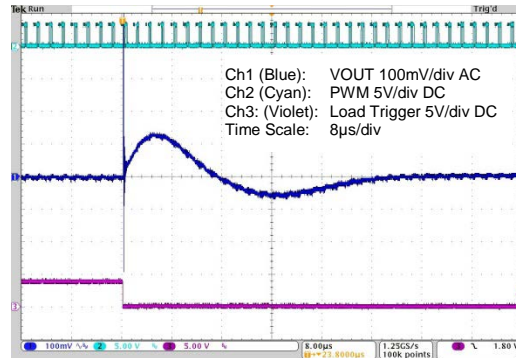
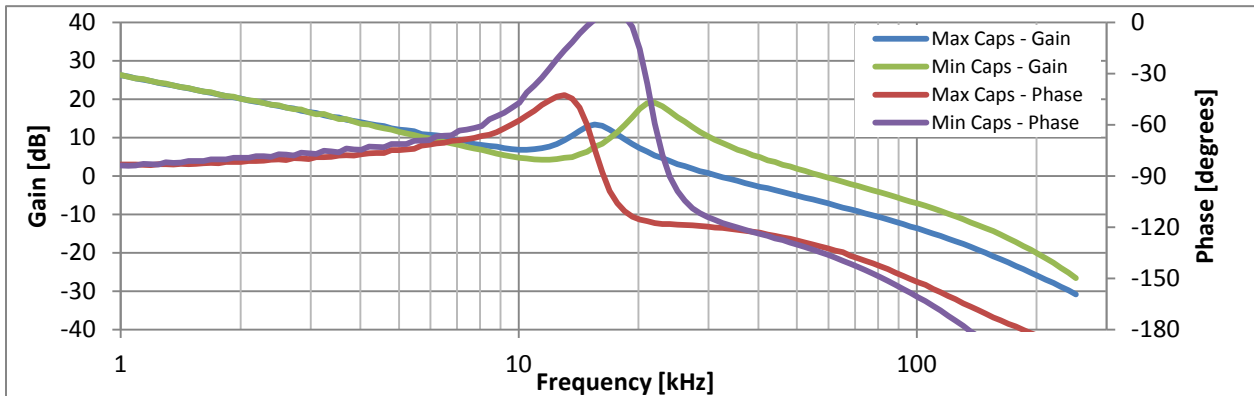


Figure 5.26 Open Loop Bode Plots for VOUT Range #2 with Capacitor Range #1



5.2.6. Typical Load Transient Response – Capacitor Range #2 – VOUT Range #2

Test conditions: $V_{IN} = 12.0V$, $V_{OUT} = 1.80V$

Minimum output capacitance: $3 \times 100\mu F/6.3V \text{ X5R} + 2 \times 47\mu F/10V \text{ X7R}$

Maximum output capacitance: $7 \times 100\mu F/6.3V \text{ X5R} + 4 \times 47\mu F/10V \text{ X7R}$

Figure 5.27 VOUT Range #2 with Capacitor Range #2 – Load Step 5 to 15A, Min. Capacitance

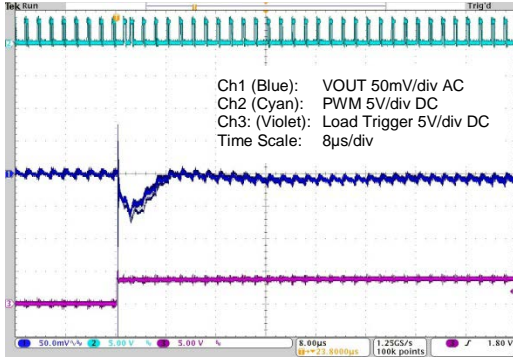


Figure 5.28 VOUT Range #2 with Capacitor Range #2 – Load Step 15 to 5A, Min. Capacitance

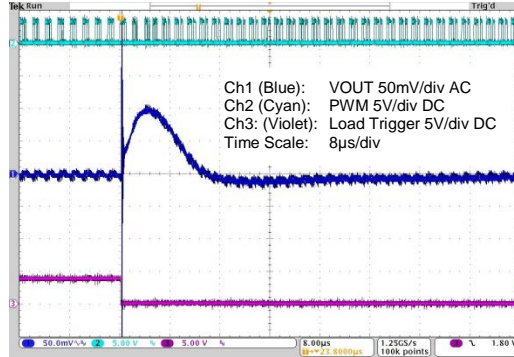


Figure 5.29 VOUT Range #2 with Capacitor Range #2 – Load Step 5 to 15A, Max. Capacitance

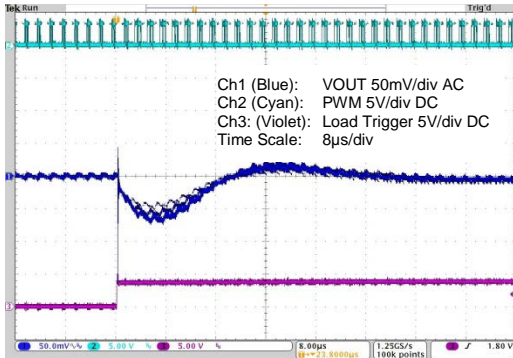


Figure 5.30 VOUT Range #2 with Capacitor Range #2 – Load Step 15 to 5A, Max. Capacitance

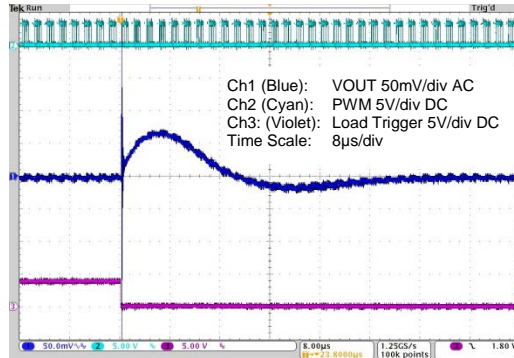
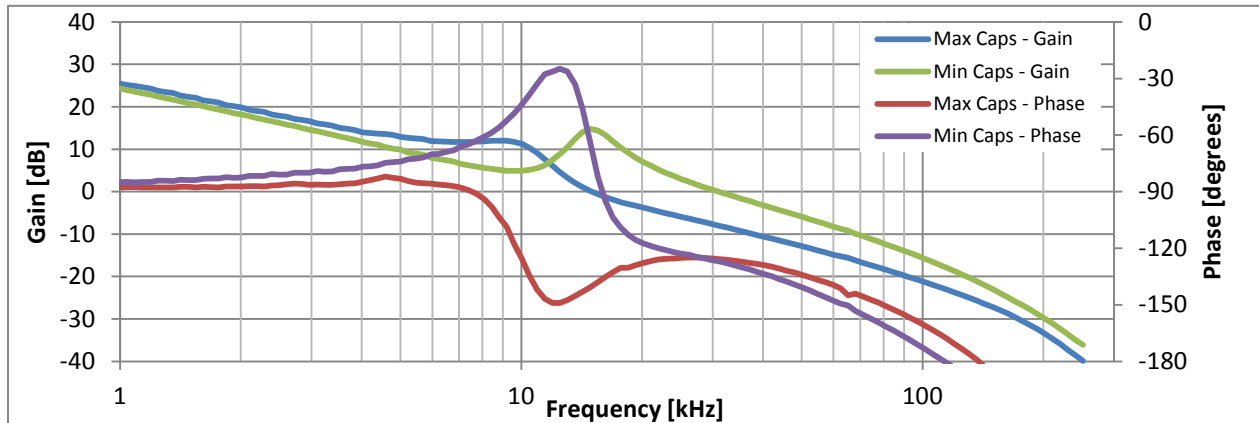


Figure 5.31 Open Loop Bode Plots for VOUT Range #2 with Capacitor Range #2



5.2.7. Typical Load Transient Response – Capacitor Range #3 – VOUT Range #2

Test conditions: $V_{IN} = 12.0V$, $V_{OUT} = 1.80V$

Minimum output capacitance: 1 x 100 μ F/6.3V X5R + 2 x 470 μ F/6.3V/7m Ω Aluminum Electrolytic Capacitor

Maximum output capacitance: 6 x 100 μ F/6.3V X5R + 5 x 470 μ F/6.3V/7m Ω Aluminum Electrolytic Capacitor

Figure 5.32 VOUT Range #2 with Capacitor Range #3 – Load Step 5 to 15A, Min. Capacitance

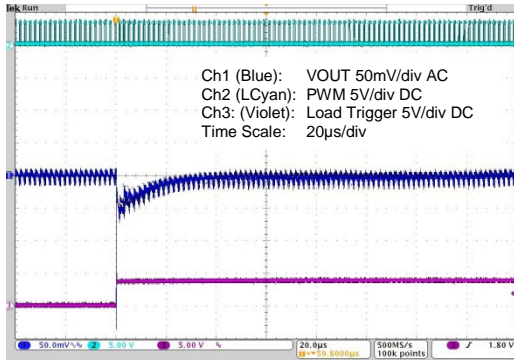


Figure 5.33 VOUT Range #2 with Capacitor Range #3 – Load Step 15 to 5A, Min. Capacitance

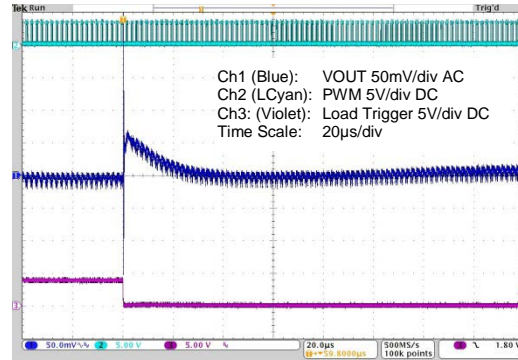


Figure 5.34 VOUT Range #2 with Capacitor Range #3 – Load Step 5 to 15A, Max. Capacitance

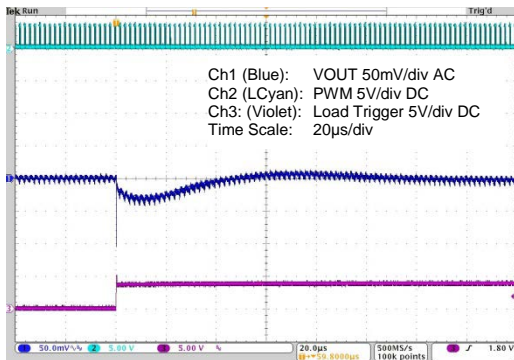


Figure 5.35 VOUT Range #2 with Capacitor Range #3 – Load Step 15 to 5A, Max. Capacitance

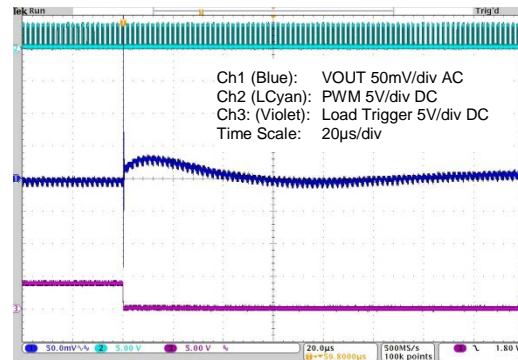
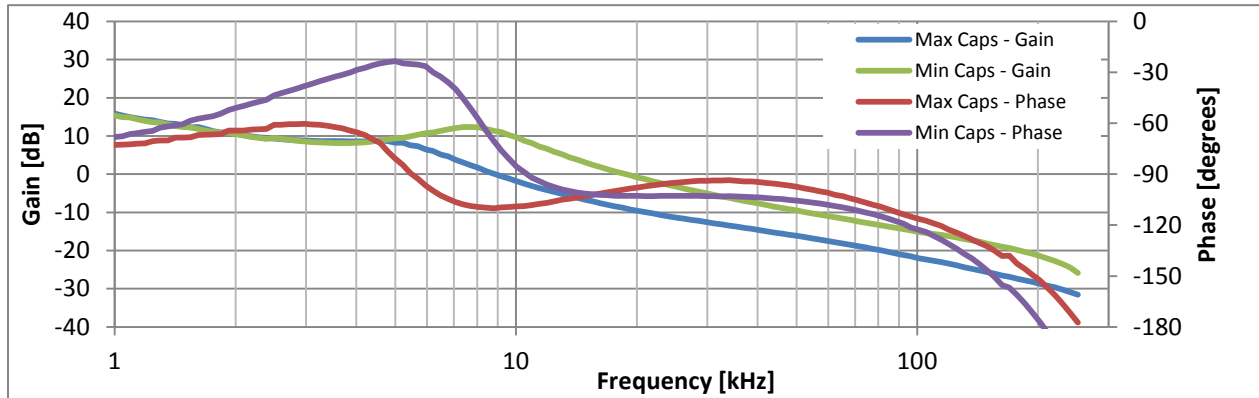


Figure 5.36 Open Loop Bode Plots for VOUT Range #2 with Capacitor Range #3



5.2.8. Typical Load Transient Response – Capacitor Range #4 – VOUT Range #2

Test conditions: $V_{IN} = 12.0V$, $V_{OUT} = 1.80V$

Minimum output capacitance: 3 x 100 μ F/6.3V X5R + 2 x 47 μ F/10V X7R + 4 x 470 μ F/6.3V/7m Ω Aluminum Electrolytic Capacitor

Maximum output capacitance: 7 x 100 μ F/6.3V X5R + 4 x 47 μ F/10V X7R + 10 x 470 μ F/6.3V/7m Ω Aluminum Electrolytic Capacitor

Figure 5.37 VOUT Range #2 with Capacitor Range #4 – Load Step 5 to 15A, Min. Capacitance

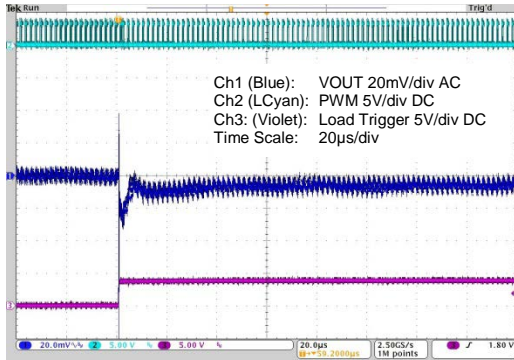


Figure 5.38 VOUT Range #2 with Capacitor Range #4 – Load Step 15 to 5A, Min. Capacitance

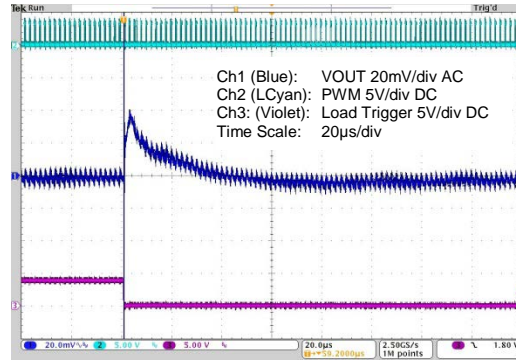


Figure 5.39 VOUT Range #2 with Capacitor Range #4 – Load Step 5 to 15A, Max. Capacitance

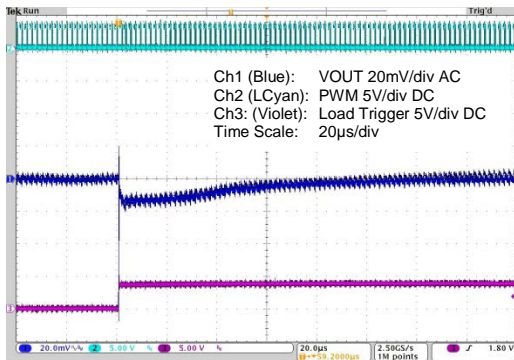


Figure 5.40 VOUT Range #2 with Capacitor Range #4 – Load Step 15 to 5A, Max. Capacitance

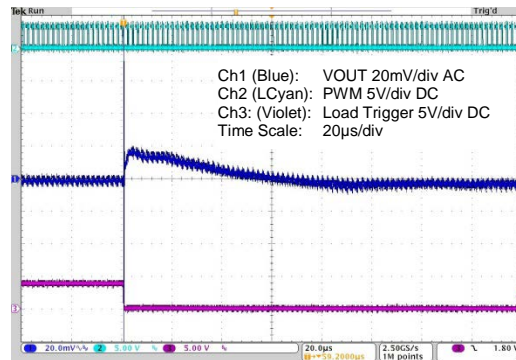
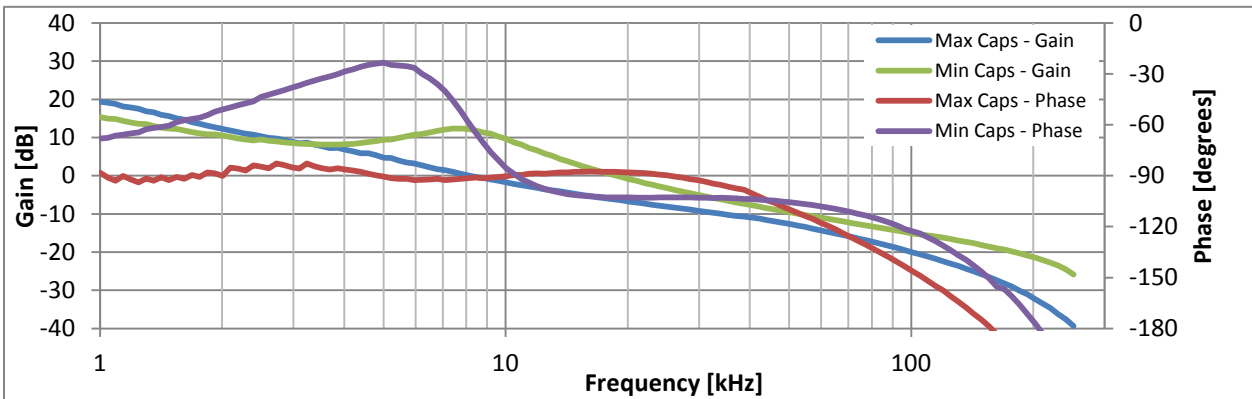


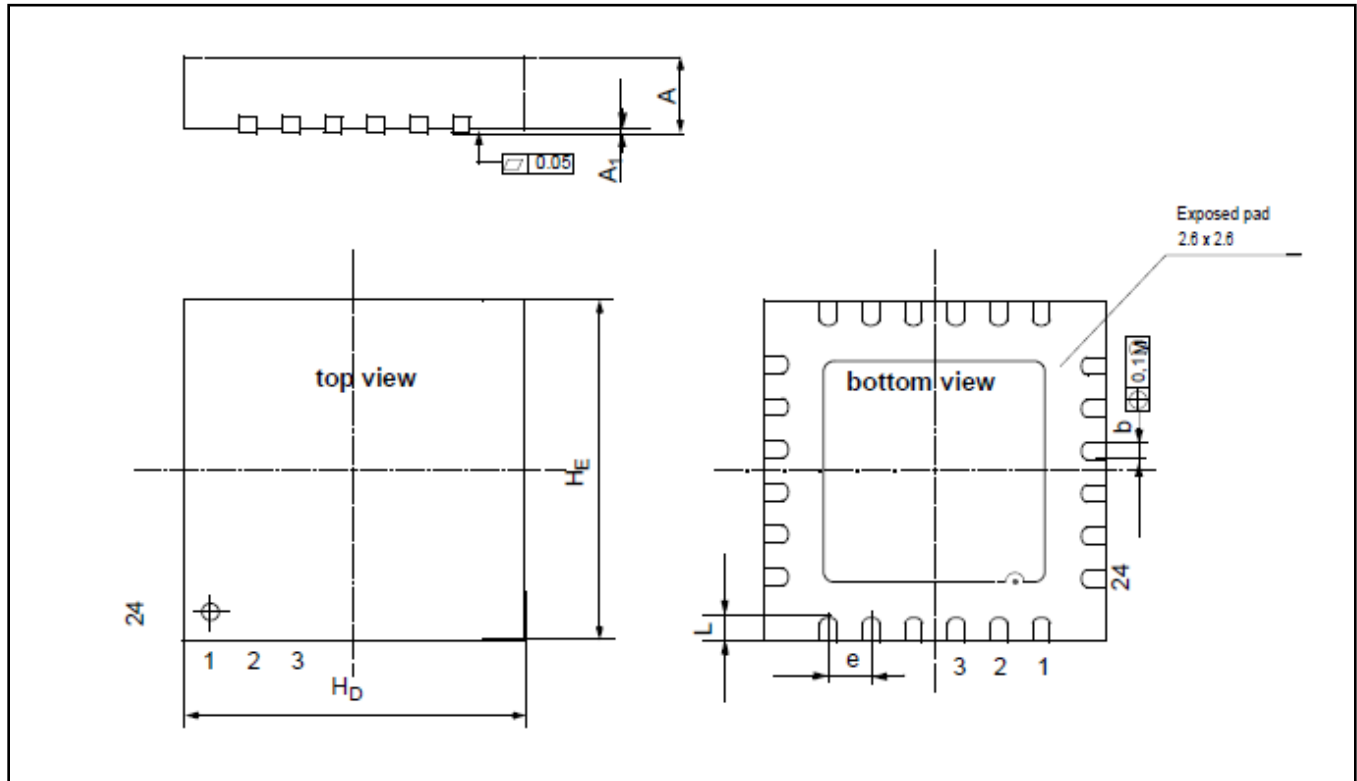
Figure 5.41 Open Loop Bode Plots for VOUT Range #2 with Capacitor Range #4



6 Mechanical Specifications

Based on JEDEC MO-220. All dimensions are in millimeters.

Figure 6.1 Package Drawing



| Dimensions [mm] | Min | Max |
|-----------------|-------------|------|
| A | 0.8 | 0.90 |
| A ₁ | 0.00 | 0.05 |
| b | 0.18 | 0.30 |
| e | 0.5 nominal | |
| H _D | 3.90 | 4.1 |
| H _E | 3.90 | 4.1 |
| L | 0.35 | 0.45 |

7 Ordering Information

This product is sold under a limited license from PowerOne, Inc. related to digital power technology as set forth in U.S. Patent 7000125 and other related patents owned by PowerOne, Inc. This license does not extend to stand-alone power supply products.

| Sales Code | Description | Package |
|----------------|---|---------|
| ZSPM1035AA1W 1 | ZSPM1035A Lead-free QFN24 — Temperature range: -40°C to +125°C | Reel |
| ZSPM8035-KIT | Evaluation Kit for ZSPM1035A: PMBus™ Communication Interface — Pink Power Designer™ GUI for kit can be downloaded from the IDT web site at www.IDT.com/ZSPM1035A | Kit |

8 Related Documents

| Document |
|---|
| <i>ZSPM1035A Feature Sheet</i> |
| <i>ZSPM8035-KIT Evaluation Kit Description</i> |
| <i>ZSPM1035A Pink Power Designer™ Graphic User Interface (GUI) User Guide</i> |
| <i>ZSPM1035A Application Note—Programming and Calibration</i> |

Visit the ZSPM1035A product page (www.IDT.com/ZSPM1035A) or contact your nearest sales office for the latest version of these documents.

9 Glossary

| Term | Description |
|-------|--|
| ASIC | Application Specific Integrated Circuit |
| DPWM | Digital Pulse-Width Modulator |
| DCR | DC Resistance |
| DSP | Digital Signal Processing |
| FET | Field-Effect Transistor |
| FPGA | Field-Programmable Gate Array |
| GPIO | General Purpose Input/Output |
| GUI | Graphical User Interface |
| HKADC | Housekeeping Analog-To-Digital Converter |
| NVM | Non-volatile Memory |
| OT | Over-Temperature |
| OTP | One-Time Programmable Memory |

| Term | Description |
|------|----------------------------------|
| OV | Over-Voltage |
| PEC | Packet Error Correction |
| PID | Proportional/Integral/Derivative |
| POR | Power-On-Reset |
| SCR | Sub-cycle Response™ |
| SLC | State-Law Control™ |
| SPM | Smart Power Management |

10 Document Revision History

| Revision | Date | Description |
|----------|------------------|---|
| 1.00 | December 3, 2013 | First release. |
| 1.10 | February 5, 2014 | Addition of description of available reference solution on page 2. |
| 1.11 | October 15, 2014 | Correction of bias voltage for Murata power block in Figure 2.1 and Figure 5.1. Update to add PowerOne, Inc. license information. Update for contact information. |
| | January 27, 2016 | Changed to IDT branding. |

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